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A Low Power Low Voltage CMOS Based Operational Transconductance Amplifier for Biomedical Application

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Abstract: In this paper, a low power low trans-conductance operational trans-conductance amplifier (OTA) is designed for biomedical application such as the EEG and ECG. To achieve a very low trans-conductance with low power the OTA should operate in sub threshold region or weak inversion. For better linearity of the OTA, the multi-tanh doublet linearization technique is used. In this design 90nm CMOS technology is used with ±0.35V supply voltage. The linear range of the OTA is 200mV and the power dissipation is below 5nW. The trans-conductance value of the OTA is 50nS which can be tuned by varying in control voltage VC. The 3-db cutoff frequency required for ECG and EEG is 250Hz and 200Hz respectively.

Keywords: OTA, Biomedical Frequency, ECG, EEG, CMOS, Weak Inversion.

I. INTRODUCTION

The biomedical application such as ECG, EEG requires very low power designs because portable biomedical sensors are usually powered by battery. ECG and EEG are two most biomedical mapping instrument, these instruments are used to monitor functioning of two of the most important parts of the human body heart and brain. The key factor that is currently being researched around the world is the design of circuits with low power and low voltage applications [1]. Generally, it is preferred to run low voltage circuits using CMOS technology. OTA finds its application in several fields, such as gain control amplifiers, oscillators, etc. Multistage amplifiers are used to prevent unwanted output oscillations. This document proposes a design methodology for a CMOS-based operational transconductance amplifier that provides reduced power dissipation by increasing OTA performance. The goal of this work is to design an operational transconductance amplifier for biomedical ECG and EEG applications. OTA is a design required for the low-pass filter circuit that is part of the portable biomedical signal processing system to electrically monitor and record cardiac activity (ECG) and brain activity (EEG). The operational transconductance amplifier (OTA) is a widely used analog processing block. In recent years, the development of operational transconductance amplifier (OTA) with very low transconductance and improved the linearity range of the OTA which is mainly used in biomedical application circuits. Many OTA topologies have been developed to obtain a very low transconductance in some nA / V with a good linear range [7]. The demand for biomedical instruments is increasing worldwide. Low voltage and low power are the need for biomedical instruments to extend battery life. [15] The low transconductance OTA is important in the design of biomedical or low frequency filters that are used in the biomedical signal processing system. OTA is designed using multiple topologies for low power and low transconductance. In this design, the low transconductance OTA is designed with low power dissipation that operates in the weak inversion or sub threshold region is realized. To increase the linearity of the OTA circuit, the multi-tan linearization technique is used.

II. MOS GILBERT CELL DOUBLET IN WEAK INVERSION

In the weak inversion or sub threshold region, the majority carriers are replaced away from the channel region, hence we have very small density of the minority carriers. Typically, the sub threshold current lies roughly in 10^{-9} to 10^{-7} ampere range. When a MOS transistor is operating in the sub threshold region the current is given by;

$$I_{DS} = I_M \left(\frac{W}{L}\right) \exp\left(\frac{V_{GS} - V_M}{n\emptyset_t}\right)\left[1 - \exp \quad \frac{-V_{DS}}{\emptyset_t}\right] \quad (2)$$

Where, I_M is the characteristic current of order 10^{-15} to 10^{-12} amperes. [refer Anantha-P chandrakasan] V_M is upper limit of weak inversion or sub threshold in term of V_{GS} (consider with thermal voltage) for a fixed V_{BS} (in this design -0.35V). $\emptyset_t$ is thermal voltage and n is sub threshold slope factor,

$$n = \frac{C_{ox} + C_{Dep}}{C_{ox}} = \frac{1}{K} \quad \textbf{(2)}$$

C_{ox} is oxide capacitance and C_{DEP} is depletion capacitance. From eq. (1), here I_{DS} is independent of V_{DS} when $V_{DS} > 3\emptyset_t$,with less than 5% error. So, we can approximate the eq. (1) as,

$$I_{DS} = I_{Do} \left(\frac{W}{L}\right) \exp\left(\frac{V_{GS}}{n\emptyset_t}\right) \quad \textbf{(3)}$$

Where,

$$I_{Do} = I_M \exp\left(\frac{-V_M}{n\emptyset_t}\right) \quad \textbf{(4)}$$

A. Single Stage Amplifier In Sub Threshold Region Or Weak Inversion

The basic is diagram of the single stage amplifier is shown in the Fig. 1. We operate this single stage amplifier in sub threshold region and the output current of this single stage amplifier in sub threshold region is given by:

$$I_{out} = I_B \tanh\left[\frac{V_{in}}{2n\emptyset_t}\right] \quad \textbf{(5)}$$

Where, n is the sub threshold slope factor, which value is shown in eq. (2)

$I_B = i_+ + i_-$

And V_{in} is the input voltage $V_{in} = V_+ + V_-$

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = \left.\frac{k\, I_B}{2\emptyset_t}\right|_{V_{in}=0} = \frac{I_B}{\left(\frac{2\emptyset_t}{k}\right)} \quad \textbf{(6)}$$

$$V_L = \frac{2\emptyset_t}{k}$$

So,

$$G_m = \frac{I_B}{V_L} \quad \textbf{(7)}$$

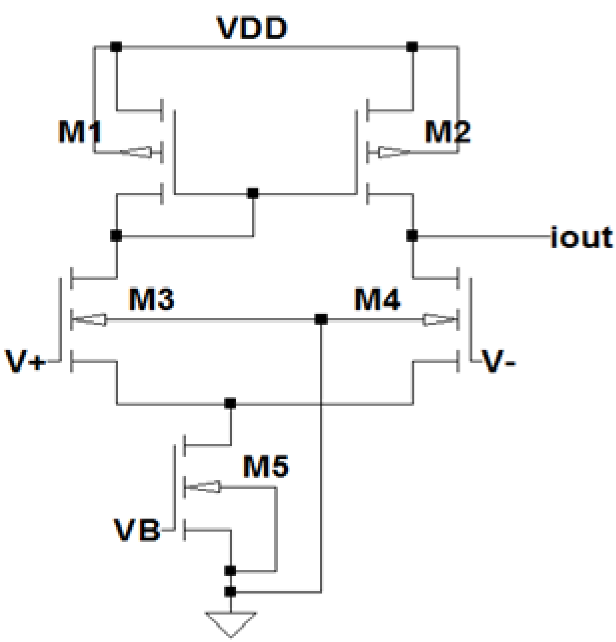

Fig.1. single stage amplifier in sub threshold region or weak inversion.

G_m is the small signal transconductance g_m of M_3 and M_4 (input transistors). If we apply $(+V_{in} / 2)$ and $(-V_{in} / 2)$, hence the output current is

$$I_{out} = g_m V_{in} \quad \textbf{(8)}$$

V_L (Linear Voltage Range) can be obtained by extrapolating the G_m slope at origin until the saturation current I_B is reached. Let, k = 0.7, $\emptyset_t$ = 26mV, then $V_L = (2\emptyset_t / k)$ = 75mV is very less. If we operate this circuit in saturation can yield more large result but power consumption increases as well as we lose common mode dc operating range. So, it is required to design a low power transconductance capable of having value of V_L (Linear Voltage Range) is more in sub threshold operation without losing signification amount of common mode dc operating range. To add more linearization we add a technique called "multi-tanh linearization".

B. Multi-tanh Doublet Technique

Gilbert Multiplier cell is used as OTA which is previously used in saturation region as a multiplier, but in sub threshold region its transconductance is defined by tanh trigonometric identity. To increase the linear range of the circuit, the multi-tanh doublet technique is used. In the Fig. 2, the differential pair represented by sets M1 – M2 & M3 – M4 shown a voltage offset with the same absolute value but in opposite direction of transfer characteristics. I_1, I_2, I_3 and I_4 are the current of transistors M_1, M_2, M_3 and M_4 respectively.

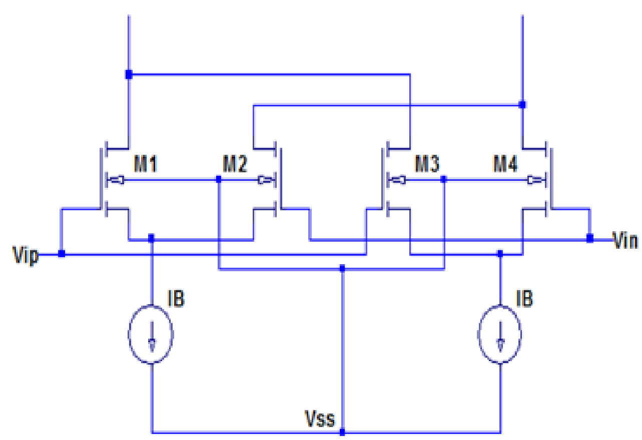

Fig.2. Multi tanh doublet linearity technique.

$$I_1 - I_2 = I_B \tanh\left[\frac{V_{in} + V_{os}}{2n\emptyset_t}\right] \quad \textbf{(9)}$$

And

$$I_3 - I_4 = I_B \tanh\left[\frac{V_{in} - V_{os}}{2n\emptyset_t}\right] \quad \textbf{(10)}$$

The output current of this circuit is given by:

$$I_{out} = (I_1 - I_2) + (I_3 - I_4) \quad \textbf{(11)}$$

Now, from using the eq. (9) and eq. (10) the final output current of the circuit is

$$I_{out} = I_B\left\{\tanh\left[\frac{V_{in} + V_{os}}{2n\emptyset_t}\right] + \tanh\left[\frac{V_{in} - V_{os}}{2n\emptyset_t}\right]\right\} \quad \textbf{(12)}$$

Using this technique we increase the linearity of the circuit and also the power consumption of the circuit is very low using this technique.

III. PROPOSED TRANSCONDUCTOR

Using the Multi-tanh doublet technique design the required low power low transconductance OTA which operates in sub threshold region. The proposed design of OTA is shown in the Fig.3. In this OTA M1-M2 and M3-M4 are the two input differential pair of the OTA connected in parallel. In which we apply the positive input voltage at M1 and M4 and negative input voltage at M3 and M4. Using multi-tanh doublet we increase the linearity of the circuit and also power consumption of circuit is very low and we also operate this circuit in sub threshold at very low supply voltage. The output current of each input transistor is shown in Fig.4.

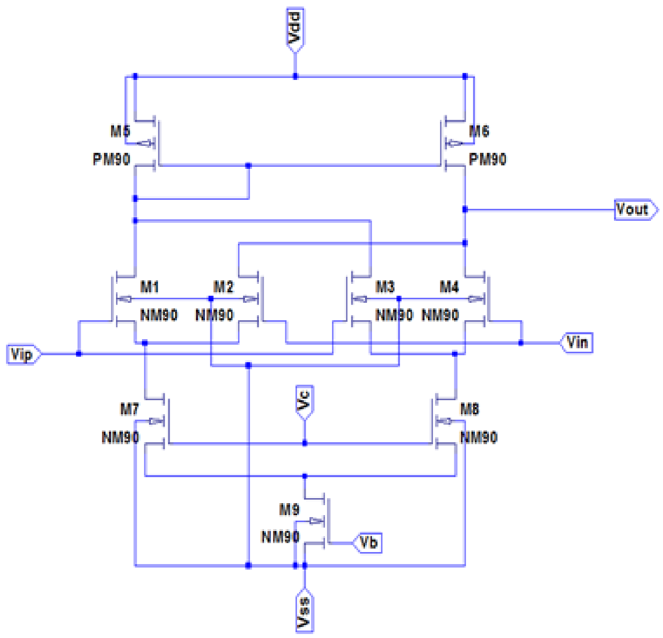

Fig.3. Proposed OTA design.

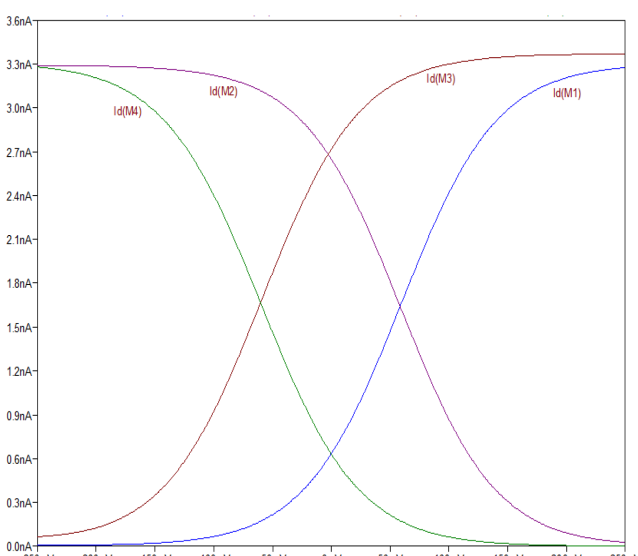

Fig.4. Output Current of Each Input transistor.

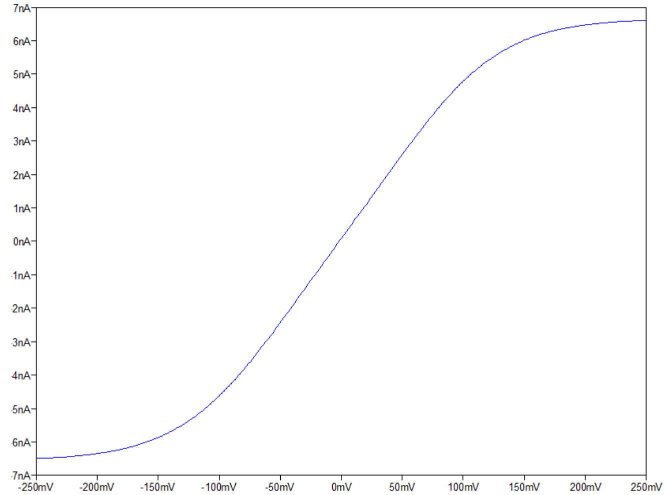

Fig.5. Overall output current of OTA.

The overall current in the OTA is -6.50nA to 6.60nA, thus the total current requirement of OTA is 13nA. The OTA output current is shown in the Fig. 5. The transconductance of the each input differential pair is 25nS and the overall transconductance of the designed OTA is 50nS.

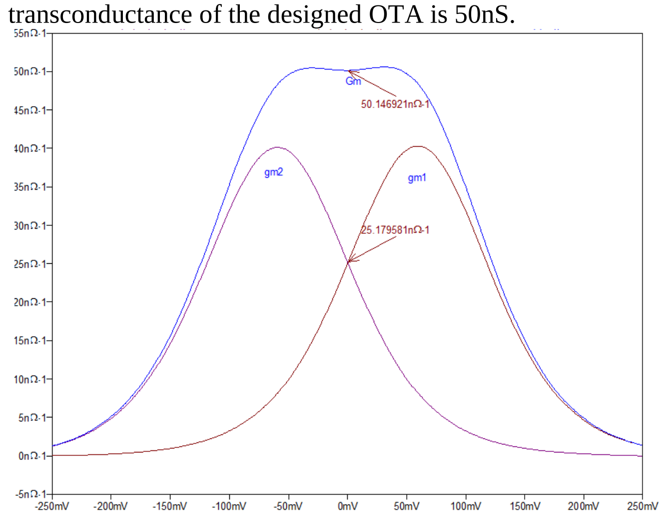

Fig.6. Transconductance of the each input differential pair and overall transconductance of the OTA.

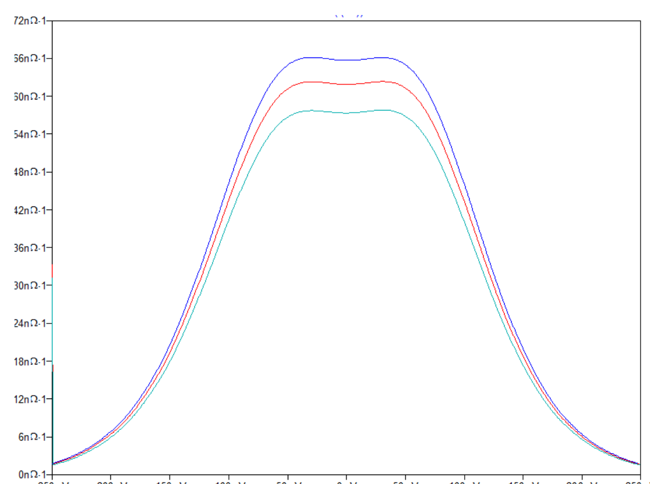

Fig.7. Variation of the Overall Transconductance by Varying Control Voltage (V_c).

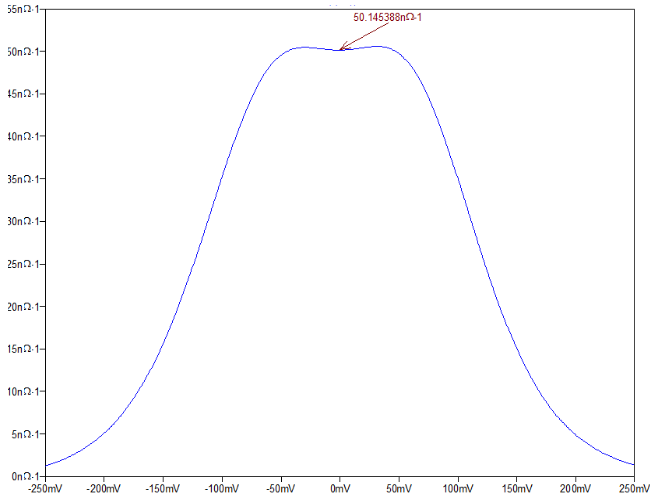

Fig.8. Overall transconductance of OTA.

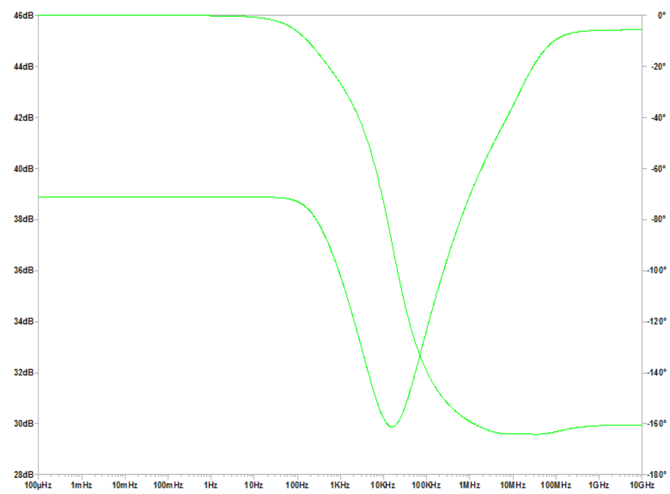

Fig. 9. Phase and Magnitude Response of the roposed OTA Design.

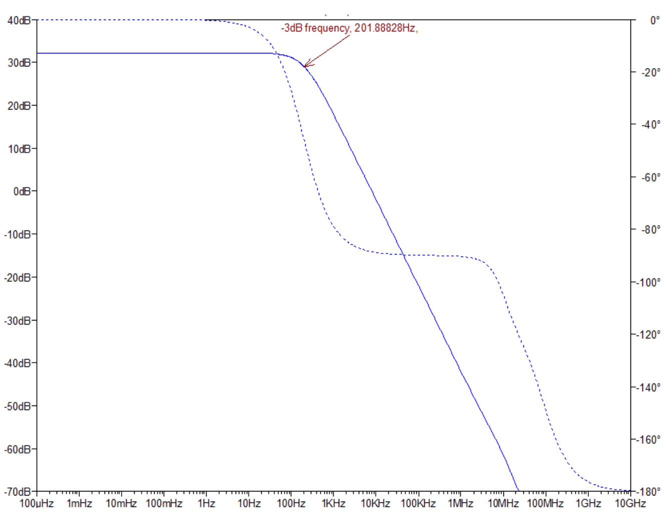

Fig.10. Frequency response of OTA.

The control voltage (V_c) is used in the OTA to control or vary the transconductance of OTA with different value of the control voltage. Using the control voltage the transconductance of the OTA is varied and can also the frequency of the filter. The variation in the transconductance by varying control voltage is shown in Fig.7. The overall transconductance of OTA is 50nS without varying the control voltage (i.e. keeping V_C fixed at -0.134V). The transconductance of the OTA is shown in the Fig.8. The magnitude of the Proposed OTA is 35.802074dB and the phage of the OTA is 26.5° and also we get the Group delay of the proposed OTA design is 31.354321µs. This is shown in the Fig.9. The AC response shown in Fig.10 is obtained by adding a 1pF load capacitor at the output terminal of the OTA.

TABLE I: Transistor Demission of the Proposed OTA Design

Transistor No.	W/L (µm / µm)	Aspect Ratio
M1 , M4	0.09 / 0.09	1
M2 , M3	0.35 / 0.09	4
M5 , M6	0.12 / 0.30	0.4
M7 , M8 , M9	1.5 / 1	1.5

TABLE II: Summary of OTA Results

Parameters	Value
CMOS Technology	90nm
Supply Voltage	±0.35V
Power Consumption	4.7nW
Overall Current	13.2nA
Magnitude	35.802074dB
Phase Margin	26.5°
Group Delay	31.354321µs
Tranconductance	50nS
Transconductance Tuning Method	By varying Control Voltage (V_C)

TABLE III: Comparison Proposed Work with Previous Work

	[2]	[7]	[10]	[4]	[11]	This Work
CMOS Technology (µm)	0.18	0.18	0.18	0.09	0.18	0.09
Supply Voltage (V)	0.4	0.85	1	1.1	1	±0.35
Power Dissipation (µW)	0.38 6	1.2	17	712	7.24	0.0047
Gain (dB)	91	__	40.3-81.02	60	67.8 1	35.8
Load Capacitor (pF)	15	__	2	10		1
Gm	10.5	2.5	__	3800		50
Phase Margin	66°	__	__	45°	45.9°	26.5°

IV. CONCLUTATION

In this paper, the low power low transconductance OTA is designed for biomedical application such as EEG and ECG. This OTA is operated in sub threshold region and it is designed using multi-tanh linearization technique. In this design 90nm CMOS technology is used with ±0.35V supply voltage. The transconductance of the OTA is 50nS which is varying using the control voltage V_C. The Gain of the

Proposed OTA is 35.802074dB and the phage of the OTA is 26.5°. The power consumption of the OTA is 4.7nW and the overall current of the OTA is 13.2nA.

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