International Journal of Scientific Engineering and Technology Research

ISSN 2319-8885
Vol.06,Issue.24
July-2017,
Pages:4724-4732

www.ijsetr.com

Five-Level Dual-Buck Full-Bridge Inverters for Grid-Tied Applications

GURAJALA HARIKA[1], CH. JHANSILAKSHMI[2], L. KISORE[3]

[1]PG Scholar, Sreekavitha Engineering College, Khammam, Telanagana, India.
[2]Assistant Professor, Sreekavitha Engineering College, Khammam, Telanagana, India.
[3]Associate Professor, Sreekavitha Engineering College, Khammam, Telanagana, India.

Abstract: In this paper, the detailed derivation process of two five-level full-bridge topology generation rules are presented and explained. One is the combination of a conventional three-level full-bridge inverter, a two-level capacitive voltage divider, and a neutral point clamped branch. The other method is to combine a three-level half-bridge inverter and a two-level half-bridge inverter. Furthermore, in order to enhance the reliability of existing five-level DBFBI topologies, an extended five-level DBFBI topology generation method is proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter; thus, a family of five-level DBFBI topologies with high reliability is proposed. The operation modes, modulation methods, and control strategies of the series-switch five-level DBFBI topology are analyzed in detail. The power device losses of the three-level DBFBI topology and five-level DBFBI topologies, with different switching frequencies, are calculated and compared. Both the relationship between the neutral point potential self-balancing and the modulation index of inverters are revealed.

Keywords: Dual-Buck Inverter, Efficiency, Grid-Tied Inverter, Multilevel Inverter, Power Density.

I. INTRODUCTION

The demand for renewable generation has increased significantly over the pastyears because of the considerations on fossil fuel shortage and greenhouse effect. Among various types of renewable generation, photovoltaic generation, wind generation, and fuel cells have been widely utilized [1]–[5], and the grid-tied inverters are key elements in renewable generation systems to interface the renewable sources and the utility grid. Therefore, they should be careful designed to achieve high efficiency and high power density. Power MOSFETs have some attractive advantages, such as fast switching, lowswitching loss, and resistive conduction voltage drop. The switching frequency of the power converters using MOSFETs can be higher than that of the power converters using insulated-gate bipolar transistors (IGBTs), which benefits for reducing current ripples and the size of passive components. However, since the reverse recovery characteristic of the body diodes is poor, power MOSFETs cannot be used in conventional H-bridge inverters. In order to utilize the advantages of MOSFETs, soft-switching techniques are adopted conventionally [6]. However, additional auxiliary switches, passive components, and more gate driving circuits are required in the soft-switching inverter, which lowers the reliability and increases the cost and complexity. In dual-buck inverters, no reverse recovery problem occurs in the freewheeling mode, since the independent freewheeling diode has excellent reverse recovery characteristic. In addition, power MOSFETs are used in dual-buck inverters.

Therefore, the dual-buck inverter is an attractive solution to achieve high efficiency for low-power grid-connected applications. Many dual-buck inverter topologies have been developed in recent years [7]–[15], and some of them are utilized as gridtied inverters.

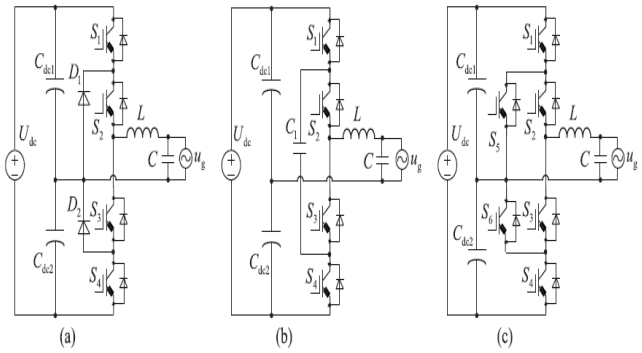

Fig 1. Three popular topologies of H-bridge multilevel inverters. (a) DNPC. (b) FCC. (c) ANPC.

Two filter inductors are required in single-phase dual-buck inverters, and both of the inductors are operating at each half cycle of the utility grid alternately, which increases the size and weight of the converter. Hence, the power density of conventional two-level and three-level dual-buck inverters needs to be improved. The multilevel technique is an effective way to achieve high power density. However, the number of power switches used in the multilevel inverter is more than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is much more

complicated. Thus, the tradeoff between the performance and the hardware cost should be considered in the design of multilevel inverters [16]. There are three widely used topologies of single-phase multilevel inverters, as shown in Fig1, diode neutral point clamped(DNPC) multilevel inverters [17][18], flying capacitor clamped (FCC). Multilevel inverters [19], [20], and active neutral point clamped (ANPC) multilevel inverters [21].

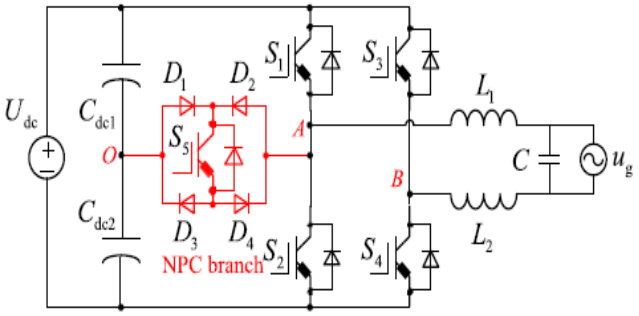

Fig 2. Simplified five-level H-bridge inverter topology [24].

The basic concept of the above three multilevel topologies is to use smaller rating power devices to generate appreciable high-level output voltage waveforms. However, conventional multilevel inverters require a large number of power devices and auxiliary dc links when the output voltage levels are higher than three-level. A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the conventional full-bridge inverter [13], [14], as shown in Fig2. Compared with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly [14]. Therefore, for the low-voltage (less than 1000V) applications, this five-level H-bridge inverter topology is a better option than conventional multilevel inverter topologies. It is regarded as one of the best solutions for grid-tied inverters as well [16]. In[14] the issue of neutral point (NP) potential balancing was discussed as well, and the NP potential self balancing of two capacitors was considered to be automatically realized. However, the NP potential self-balancing of five-level full-bridge inverters is related to the modulation index. On the other hand, three topologies of five-level dual-buck full-bridge inverters (DBFBIs) were proposed in [27], as shown in Fig3. However, the derivation process of the proposed topologies has not been explained in detail, and the topology generation rules can also be extended.

Furthermore, both the efficiency and the total harmonic distortion (THD) performance of the presented three five-level DBFBI topologies have never been analyzed and compared. In this paper, the detailed derivation processes of two fivelevel full-bridge topology generation rules are presented and explained. An extended topology generation method is proposed for generating five-level DBFBI topologies, and a family of five-level DBFBI topologies with high reliability is derived. Furthermore, the relationship between the NP potential self balancing and the modulation index of inverters is revealed.

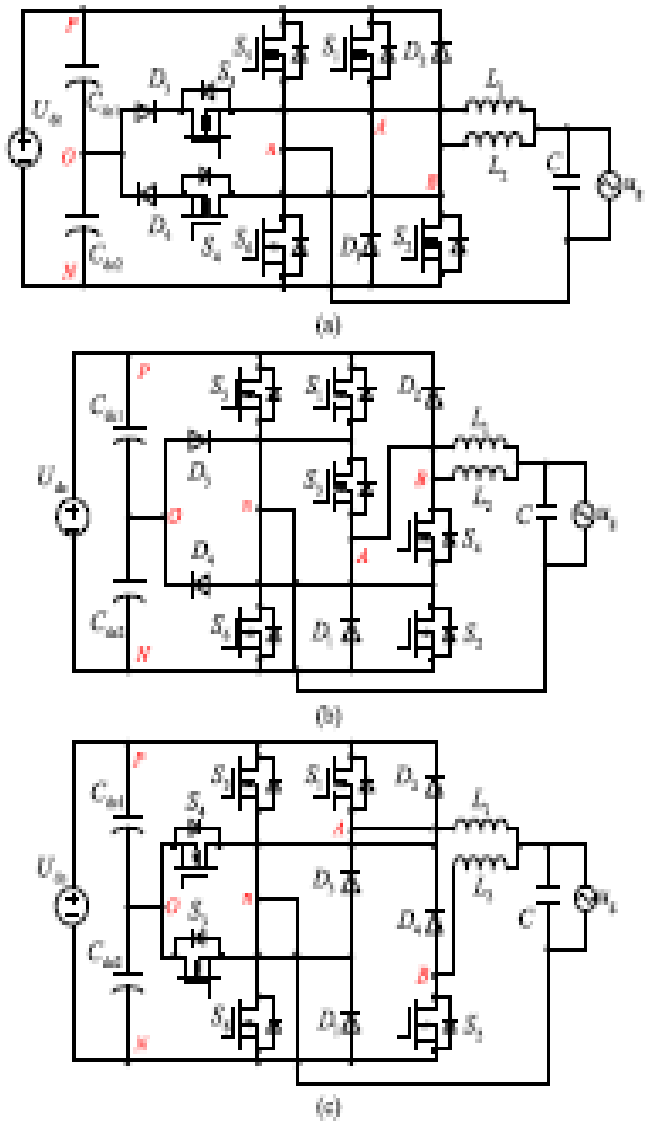

Fig 3. Three topologies of five-level DBFBIs proposed in [7]. (a) NPC fivelevel DBFBI. (b) Series-switch five-level DBFBI. (c) Series-diode five-level DBFBI.

This paper is organized as follows. In Section II, two topology generation rules of the five-level DBFBI topologies are presented and explained in detail. An extended topology generation method is proposed, and a family of five-level DBFBI topologies with high reliability is generated. In Section III, the series-switch five-level DBFBI topology is taken as an example for analysis in terms of the operation principle and the modulation method. The issue of NP potential balancing is discussed as well. In Section IV, the calculation process of power devices losses is presented, and the power devices losses comparison between the five-level DBFBI topology and the three-level DBFBI topology is given.

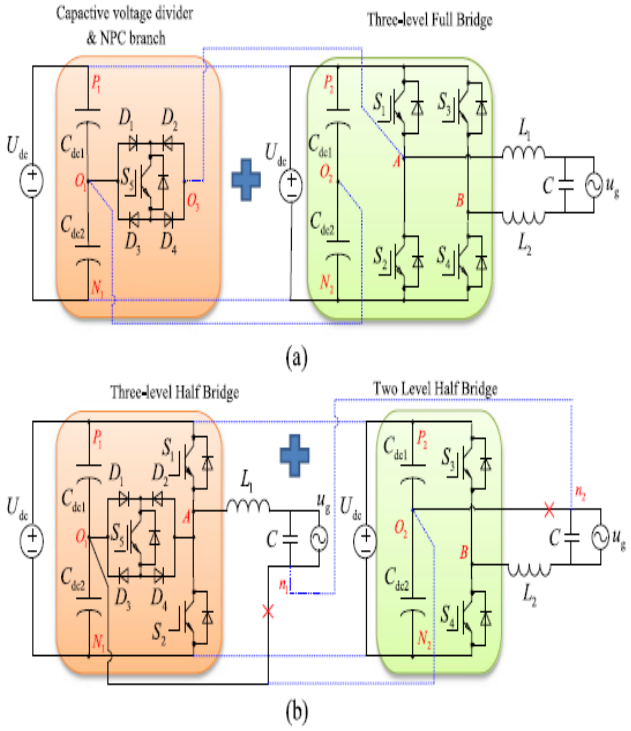

Fig 4. Topology generation rules of the simplified five-level H-bridge inverter(a) Three-level full-bridge inverter combined with a two-level capacitive voltage divider and an NPC branch. (b) Three-level half-bridge inverter combined with a two-level half-bridge inverter.

II. FAMILY OF FIVE-LEVEL DBFBIS DERIVED BY TOPOLOGY GENERATION RULES

A. Review of Topology Generation Rules

From Fig. 2, the NPC branch is formed by the switch S5 and four diodesD1–D4 . The node of the left arm A is connected with the node O (NP of the dc link) through the NPC branch. The topology generation rules of the simplified five-level H-bridge inverter can be summarized as follows.

Rule#1: The conventional three-level full-bridge inverter is combined with a two-level capacitive voltage divider and an NPC branch, as shown in Fig. 4(a). The nodes of the capacitive voltage divider P1 , N1 , and O1 are connected to the nodes of the three-level full-bridge inverter, P2 ,N2 , andO2 , respectively. The node of the NPC branch O3 is connected to the node of the three-level full-bridge inverter A. Finally, the redundant capacitors Cdc1 and Cdc2 are removed. Hence, the simplified five-level H-bridge inverter has been obtained. This topology generation rule is presented in [24] and can be applied to generate any number of voltage levels as well.

Rule#2: The simplified five-level H-bridge inverter can also be constructed by combining a three-level half-bridge inverter (Conergy topology) and a two-level half-bridge inverter, as shown in Fig. 4(b). The nodes of the three-level half-bridge inverter, P1, N1 , and O1 , are connected to the nodes of the twolevel half-bridge inverter, P2 , N2 , and O2 , respectively. The node of the three-level half-bridge inverter O1 is disconnected from the node of the utility grid n1. The node of the two-level half-bridge inverter O2 is disconnected from the node of the utility grid n2. Then, the nodes n1 and n2 are connected with each other. Hence, the simplified five-level H-bridge inverter topology can be generated by two topology generation methods, and this derivation process of the simplified five-level H-bridge inverter topology was not presented in [7].

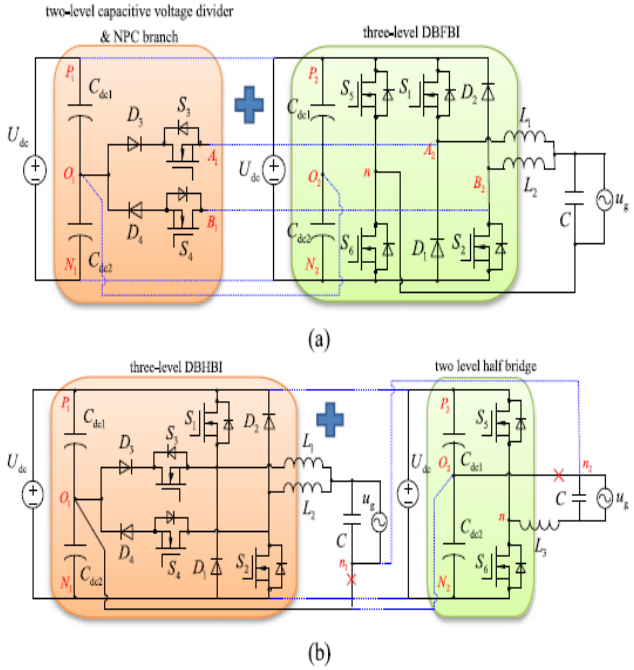

Fig 5. Topology generation rules of the proposed NPC five-level DBFBI topology (a) Three-level DBFBI combined with a two-level capacitive voltage divider and an NPC branch. (b) Three-level DBHBI combined with a two-level half-bridge inverter.

B. NPC Five-Level DBFBI Topology

By employing the topology generation rule #1, a three-level DBFBI topology is combined with a two-level capacitive voltage divider and an NPC branch, as shown in Fig. 5(a). The nodes of the capacitive voltage divider, P1 , N1 , and O1 , are connected to the nodes P2 , N2 , and O2 , respectively. The node of the NPC branch A1 is connected to the node of the three-level DBFBI A2. The node of the NPC branch B1 is connected to the node of the three-level DBFBI B2. Then, the redundant capacitors, Cdc1 and Cdc2, can be removed. As a result, an NPC five-level DBFBI topology is generated, as shown in Fig3. On the other hand, a three-level DBFBI can be combined with a two-level half-bridge inverter by employing the topology generation rule #2, as shown in Fig. 5(b). The nodes of the three level DBHBI, P1, N1, and O1, are connected to the nodes P2, N2, and O2, respectively. The node of the three-level DBHBI O1 is disconnected from the node of the utility grid n1. The node of the two-level half-bridge inverter O2 is disconnected from the node of the utility grid n2 .

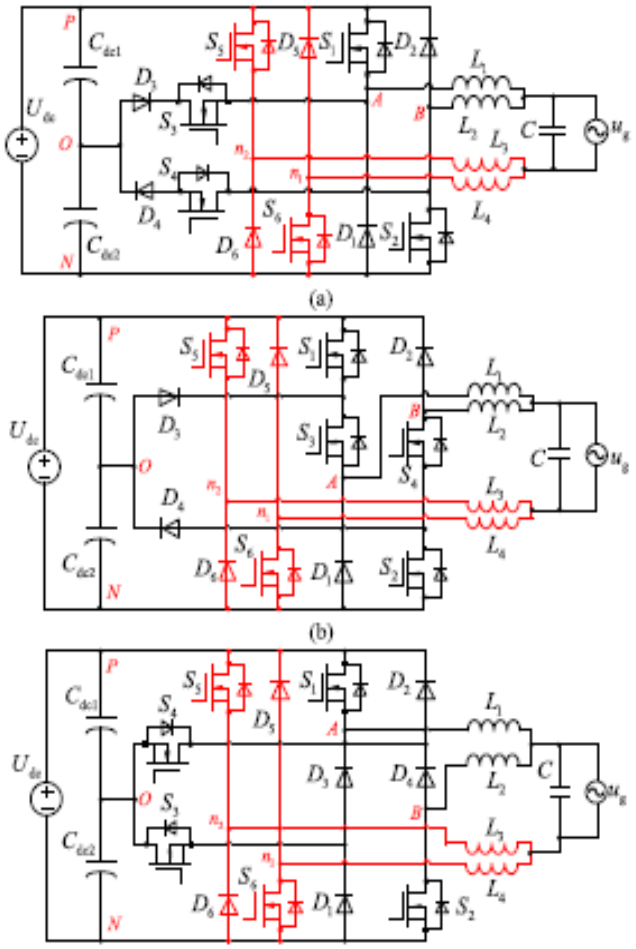

Fig 6. Three topologies of five-level DBFBIs with high reliability. (a) NPC five-levelDBFBI. (b) Series-switch five-levelDBFBI. (c) Series-diode five-level DBFBI.

Then, the nodes n1 and n2 are connected to each other. The redundant capacitors Cdc1 and Cdc2 and the redundant inductor L3 are removed. Therefore, the NPC five-level DBFBI topology can be derived from the two generation rules mentioned above. Compared with the three-level DBFBI topology [part of Fig. 5(a)], there are two additional switches and two additional diodes in the proposed NPC five-level DBFBI topology.

C. Extended Topology Generation Rule and the Other Five-Level DBFBI Topologies

In order to enhance the reliability of five-level DBFBI topologies, the two-level half-bridge inverter can be replaced by a two-level dual-buck half-bridge inverter. As a result, a family of five-level DBFBI topologies with high reliability is generated, as shown in Fig. 6. The NPC five-level DBFBI topology with high reliability, as shown in Fig. 6(a), is derived from an NPC three-level DBHBI combined with a two-level dual-buck half-bridge inverter. The series-switch five-level DBFBI topology with high reliability, as shown in Fig. 6(b), is derived from a series-switch three level DBHBI combined with a two-level dual-buck half-bridge inverter. Similarly, the series-diode five-level DBFBI, as shown

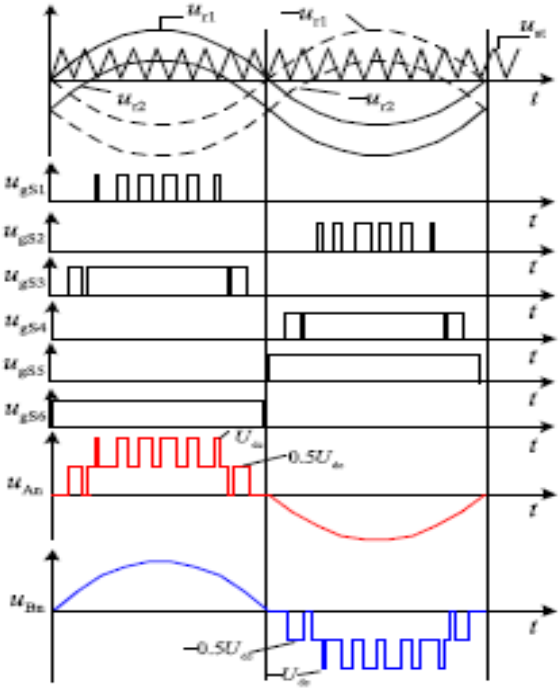

Fig 7. Key waveforms of the series-switch five-level DBFBI topology. in Fig. 6(c), is derived from a series-diode three-level DBHBI combined with a two-level dual-buck half-bridge inverter.

Therefore, a family of five-level DBFBI topologies with high reliability can be generated by employing the extended topology generation rule. Although the proposed high-reliability fivelevel DBFBI topologies are different from the topologies proposed in [27], the modulation methods and the operation modes are similar. The total inductance of split inductors (L1 and L4) in high reliability five-level DBFBI topologies is the same as that of the inductor L1 in five-level DBFBI topology. However, since there are two additional diodes, the hardware cost of the proposed high reliability topologies is higher. Therefore, the following analyses on switching states, NP potential balancing, and power devices losses are conducted based on the five-level DBFBI topologies presented in [27].

III. ANALYSIS ON THE SERIES-SWITCH FIVE-LEVEL DBFBI TOPOLOGY

A. Switching State Analysis

The series-switch five-level DBFBI topology is taken as an example for detailed analysis. The key waveforms of the series switch five-level DBFBI are shown in Fig. 7. Two reference signals ur1 and ur2 are compared with a carrier signal ust to produce pulse width modulation signals for the switches. ugS1–ugS6 represent the gate drive signals of power switches S1 to S6 . In order to avoid the shoot-through problem, the dead time has been set within the drive signals of the switches S5 and S6. uAn represents the voltage difference between the node A and node n, and uBn is the voltage difference between the node B and node n. Two filter inductors L1 and L2 are operating at each half cycle of

the utility grid alternately. Therefore, uAB−n is defined as the output levels of the DBFBI topologies, and uAB−n is represented as

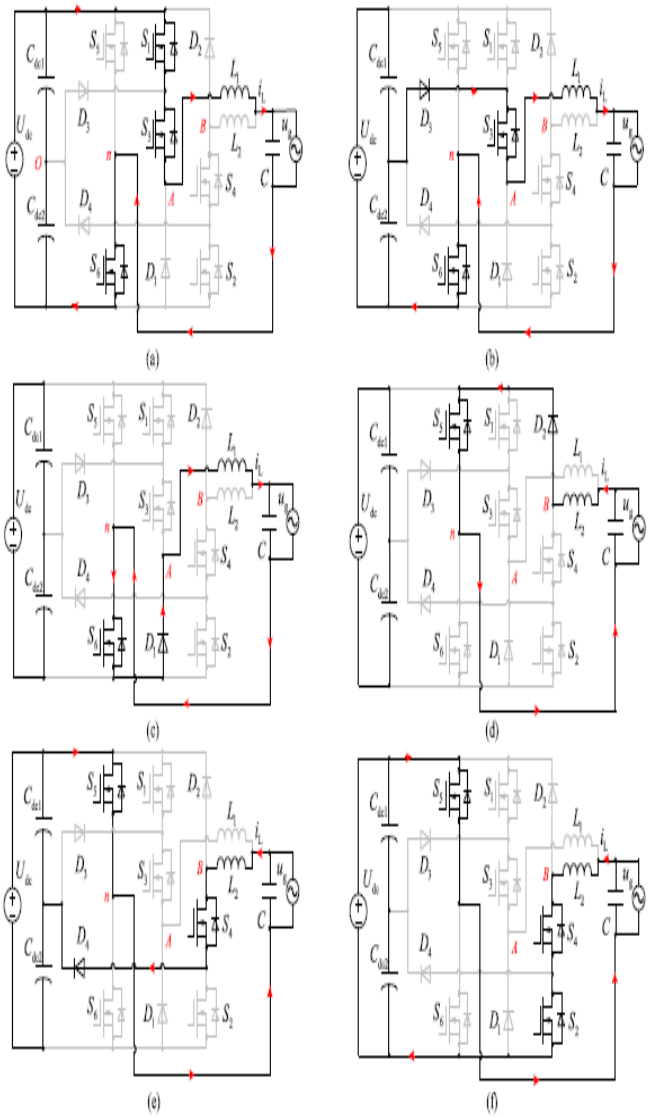

Fig 8. Equivalent circuits of switching state. (a) State #1. (b) State #2. (c) State #3. (d) State #4. (e) State #5. (f) State #6.

$$u_{\mathrm{AB-n}} = u_{\mathrm{An}} + u_{\mathrm{Bn}} - u_g. \tag{1}$$

On the other hand, the series-switch five-level DBFBI topology is operating with unity power factor. In order to avoid the inductor current distortion, at the beginning of the positive half cycle of the utility grid, the switches S1 , S3 , and S6 are turned ON at the same time. At the end of the positive half cycle, the switch S3 is turned OFF before the switch S6 , and the current of inductor L1 decreases to zero naturally. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S2 , S4 , and S5 are turned ON at the same time. At the end of the negative half cycle, the switch S4 is turned OFF before the switch S5 , and the current of inductor L2 decreases to zeronaturally. Since the series-switch five-level DBFBI topology is digitally controlled, this modulation method is easy to implement. Furthermore, it is also suitable for the NPC five-level DBFBI topology, the series-diode five-level DBFBI topology, and the family of five-level DBFBI topologies with high reliability. The series-switch five-level DBFBI has six operation modes, which are shown in Fig. 8.

1) State #1 [Refer to Fig. 8(a)]: Maximum positive output, uAn = Udc. There is no current flowing through the inductor L2 ; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = Udc. S1 , S3 , and S6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 8(a). The reverse blocking voltage on D3 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to Udc. The drain–source voltage on S5 is equal to Udc. During this state, the inductor current iL1 increases linearly

$$L_1 \frac{di_{L1}}{dt} = U_{\mathrm{dc}} - u_g. \tag{2}$$

2) State #2 [Refer to Fig. 8(b)]: Half-level positive output, uAn = 0.5Udc. There is no current flowing through the inductor L2 ; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = 0.5Udc. S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(b). The drain–source voltage on S1 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly when the voltage of the utility grid is higher than 0.5Udc

$$-L_1 \frac{di_{L1}}{dt} = \frac{U_{\mathrm{dc}}}{2} - u_g. \tag{3}$$

The inductor current iL1 increases linearly when the voltage of the utility grid is lower than 0.5Udc

$$L_1 \frac{di_{L1}}{dt} = \frac{U_{\mathrm{dc}}}{2} - u_g. \tag{4}$$

3) State #3 [Refer to Fig. 8(c)]: Zero output at the positive half period of the utility grid, uAn = 0. There is no current flowing through the inductor L2 ; thus, the voltage on the inductor L2 is equal to zero, and uBn = ug > 0. As a result, uAB−n = 0.S6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(c). Both the drain–source voltages on S1 and S3 are equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -u_g. \tag{5}$$

4) State #4 [Refer to Fig. 8(d)]: Zero output at the negative half period of the utility grid, uBn = 0. There is no current flowing through the inductor L1 ; thus, the voltage on the inductor L1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = 0.S5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(d). Both the drain–source voltages on S2 and S4 are equal to 0.5Udc. During this state, the inductor current iL2 increases linearly

$$L_2 \frac{di_{L2}}{dt} = -u_g. \tag{6}$$

5) State #5 [Refer to Fig. 8(e)]: Half-level negative output, uBn = −0.5Udc. There is no current flowing through the inductorL1 ; thus, the voltage on the inductorL1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = −0.5Udc. S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(e). The drain–source voltage on S2 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to 0.5Udc. During this state, the inductor current iL2 decreases linearly when the voltage of the utility grid is lower than 0.5Udc

$$-L_2\frac{di_{L2}}{dt}=-\frac{U_{\rm dc}}{2}-u_g. \tag{7}$$

The inductor current iL2 increases linearly when the voltage of the utility grid is higher than 0.5Udc

$$L_2\frac{di_{L2}}{dt}=-\frac{U_{\rm dc}}{2}-u_g. \tag{8}$$

6) State #6 [Refer to Fig. 8(f)]: Maximum negative output, uBn = −Udc. There is no current flowing through the inductor L1 ; thus, the voltage on the inductor L1 is equal to zero, and uAn = ug < 0. As a result, uAB−n = −Udc. S2 , S4 , and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 8(f). The reverse blocking voltage on D4 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to Udc. During this state, the drain–source voltage on S6 is equal to Udc. In this mode, the inductor current iL2 decreases linearly

$$-L_2\frac{di_{L2}}{dt}=-U_{\rm dc}-u_g. \tag{9}$$

Based on (2)–(9), it can be seen that the voltage jump of filter inductors is 0.5Udc, and the duty cycles of switches, S1–S4 , can be derived as

$$\begin{cases} d_{S1}=(2u_g/U_{\rm dc})-1, & u_g>0.5U_{\rm dc}\\ d_{S2}=(-2u_g/U_{\rm dc})-1, & -u_g>0.5U_{\rm dc}\\ d_{S3}=2u_g/U_{\rm dc}, & 0<u_g<0.5U_{\rm dc}\\ d_{S4}=-2u_g/U_{\rm dc}, & -0.5U_{\rm dc}<u_g<0. \end{cases} \tag{10}$$

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig. 2, the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage. Therefore, the switching loss of the presented fivelevel DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance.

B. Analysis of Voltage Stress

The maximum drain–source voltages on the switches S5 and S6 are equal to Udc. The maximum reverse blocking voltages on the diodes D1 and D2 are equal to Udc as well. The switch S1 is series connected with the switch S3 , and the switch S2 is series connected with the switch S4 . Therefore, the maximum drain–source voltages on the switches, S1, S2, S3, and S4, are equal to 0.5Udc. The maximum reverse blocking voltages on the diodes, D3 and D4 , are equal to 0.5Udc as well. The analysis process on the maximum voltage stresses of the power devices in the other five-level DBFBI topologies is similar.

C. Analysis of NP Potential Balancing

From Fig. 8, both the switching state #2 and switching state #5 affect the NP potential of input split capacitors. During State #2, the voltage of Cdc1 is increasing, and the voltage of Cdc2 is decreasing. During State #5, the voltage of Cdc1 is decreasing, and the voltage of Cdc2 is increasing. At the positive half cycle of the utility grid, the voltage variation of Cdc2 is represented as

$$\begin{cases} \Delta u_{C2-1}=\frac{-i_{C2}}{C_{\rm dc2}}(1-d_{S1})T_s, & u_g>\frac{U_{\rm dc}}{2}\\ \Delta u_{C2-2}=\frac{-i_{C2}}{C_{\rm dc2}}d_{S3}T_s, & 0<u_g<\frac{U_{\rm dc}}{2} \end{cases} \tag{11}$$

Where dS1 is the duty cycle of the switch S1 , and dS3 is the duty cycle of the switch S3. From (3), (4), (7), and (8), iL1 is calculated by uCdc2 during the positive half cycle of the utility grid, and iL2 is calculated by uCdc1 during the negative half cycle of the utility grid. Assuming that uCdc1 is lower than uCdc2, the root-mean-square value of iL1 is larger than that of iL2 . Therefore, the feedback of inductor current will have a positive dc component, and the output of the inductor current regulator has a negative dc component. The modulation signal has a negative dc component as well. Hence, both the dS1 and the dS3 become smaller at the positive half cycle of the utility grid. The sum of$\Delta uC2-1$ and$\Delta uC2-2$ are obtained as (12) shown. where Ng represents the total switching times in a grid period, and Ng is defined as

$$\begin{cases} \sum\limits_{t=Na+1}^{Ng/4}\Delta u_{C2-1}=\frac{-2T_s}{C_{\rm dc2}}\sum\limits_{t=Na+1}^{Ng/4}i_{C2}(t)(1-d_{S1}(t)), & u_g>\frac{U_{\rm dc}}{2}\\ \sum\limits_{1}^{Na}\Delta u_{C2-2}=\frac{-2T_s}{C_{\rm dc2}}\sum\limits_{1}^{Na}i_{C2}(t)d_{S3}(t), & 0<u_g<\frac{U_{\rm dc}}{2} \end{cases} \tag{12}$$

$$Ng=f_s/f_g \tag{13}$$

Where fg represents the frequency of the utility grid, and fs represents the switching frequency. Na represents the switching times in a quarter of grid period when 0 < ug < 0.5Udc, as shown in Fig. 9.
Na is defined as

$$Na=a\sin\left(\frac{U_{\rm dc}}{2U_{\rm om}}\right)\cdot\frac{2}{\pi}\cdot Ng \tag{14}$$

Where Uom is themaximum amplitude voltage of the utility grid. The modulation index of the five-level DBFBI topology can be calculated as

$$M=\frac{1}{2\sin\left(\frac{4Na}{Ng}\cdot\frac{\pi}{2}\right)}. \tag{15}$$

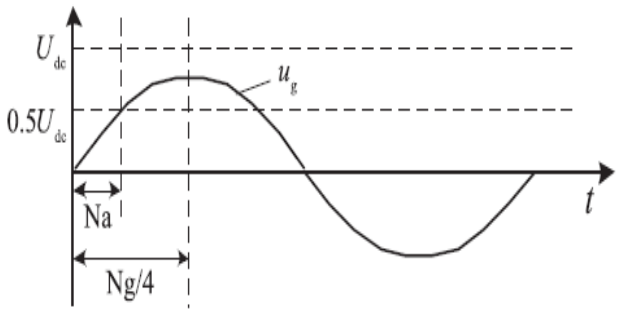

Fig 9. Sketch diagram of the switching times.

If the sum of ΔuC2−1 is higher than the sum of ΔuC2−2 , the decrease of uCdc2 becomes larger at the positive half cycle of the utility grid. Therefore, the NP potential balancing can be realized without any additional control. Contrarily, if the sum of ΔuC2−1 is smaller than the sum of ΔuC2−2 , the NP potential will be imbalanced. Assume that the voltage of the utility grid is 230 V, and the frequency of the utility grid is 50 Hz. The grid-tied power is1 kW, and the switching frequency is 40 kHz. The NP potential balancing can be realized when M> 0.56. From Fig. 10, it can be seen that when the modulation index is higher than 0.56, the divided input capacitor voltages are kept at self-balance. When the modulation index is lower than 0.56, the divided input capacitor voltages are imbalanced, and the voltages should be regulated by additional NP potential balancing mechanism, as shown in Fig. 10, where ud1 and ud2 represent the voltage of Cdc1 and Cdc2, respectively. iLr is the inductor current reference, and iLf is the feedback of the inductor current. ugff represents the feed-forward component of the utility grid voltage. Gcv is the NP potential balancing regulator, and Gci represents the inductor current regulator. The NP potential balancing is achieved by adding the output of NP potential balancing regulator and the inductor current reference.

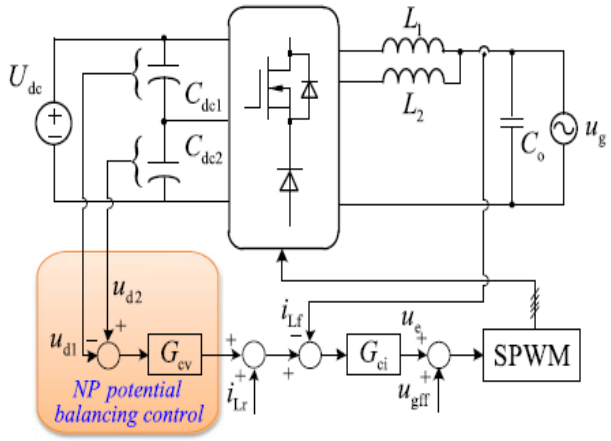

Fig 10. Control block of five-level DBFBIs.

IV. SIMULATION RESULTS

The circuit was built up to verify the feasibilities of the three-level DBFBI inverter [part of Fig. 5(a)], the NPC five-level DBFBI (see Fig. 3), the series-switch five-level DBFBI [see Fig. 3(b)],

Parameter	Value
Input voltage	350–450 V
Grid voltage	230 V/50 Hz
Grid frequency	50 Hz
Rated power	1 kW
Switching frequency	40 kHz
Three-level filter inductor L_1 & L_2	4 mH
Five-level filter inductor L_1 & L_2	2 mH
Filter Capacitor C_o	0.47 μF

The series-diode five-level DBFBI [see Fig. 3(c)], and the conventional five-level H-bridge inverter (see Fig. 2), and compare their performances. The specifications of these inverter topologies are listed in below Table . Since the lowest voltage rating of commercial SiC diodes is 600 V, only one kind of SiC diode was used in the five-level DBFBI topologies.

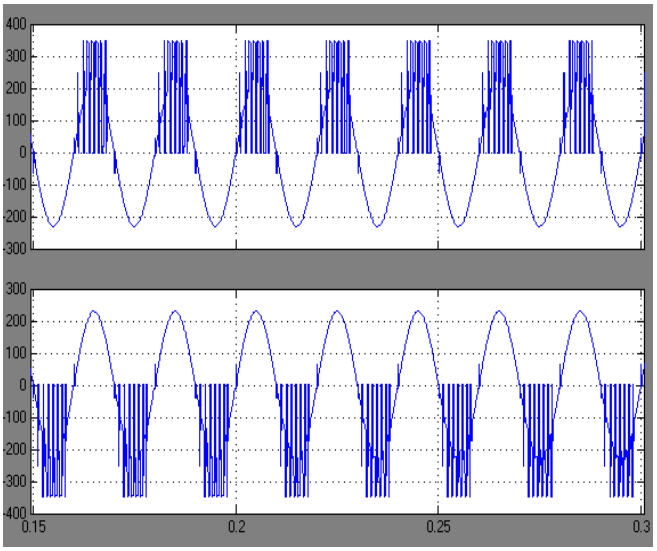

Fig 11. Simulation waveforms of the SS five-level DBFBI. uAn and uBn.

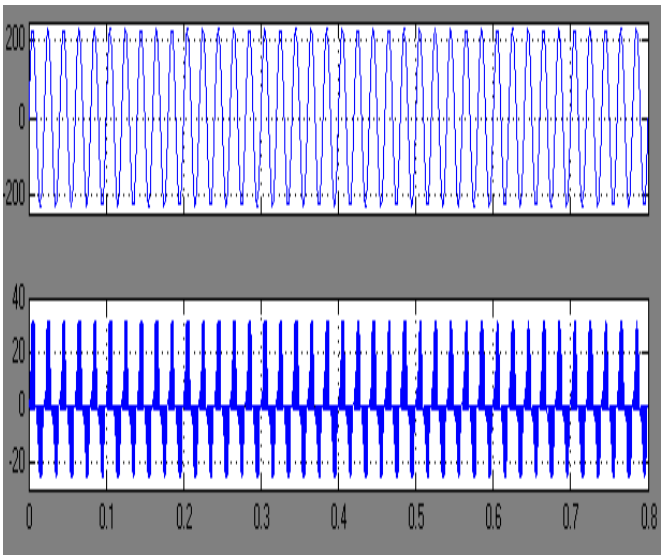

Fig 12. Simulation waveforms of the SS five-level DBFBI. Vg and Ig.

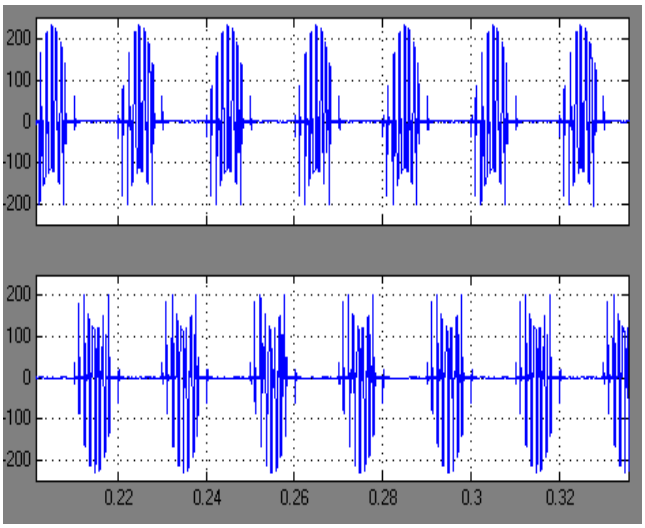

Fig 13. Simulation waveforms of the SS five-level DBFBI. Il1 and Il2.

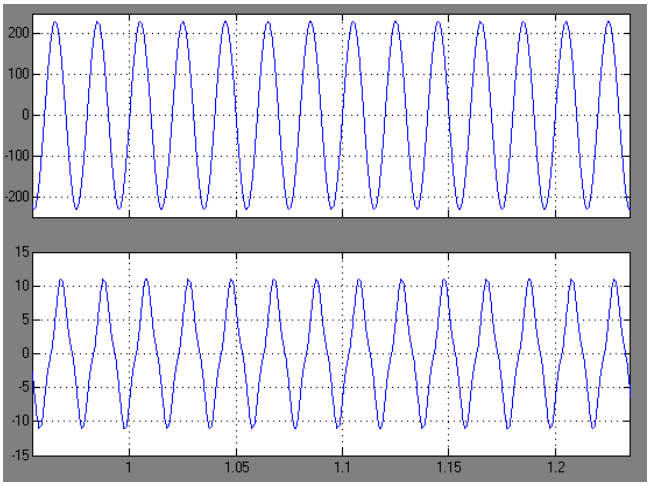

Fig 14. Simulation waveforms of the SD five-level DBFBI. Vg and Ig.

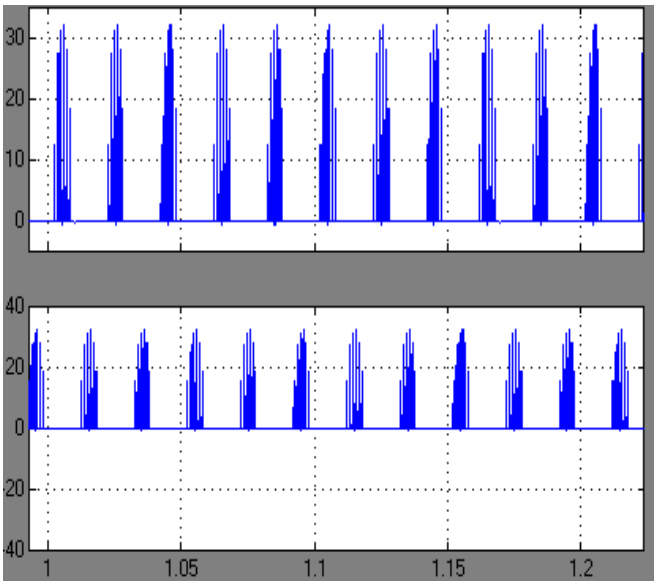

Fig 15. Simulation waveforms of the SD five-level DBFBI. Vs1and Vs2.

V. CONCLUSION

In order to enhance the reliability of five-level DBFBI topologies, an extended five-level DBFBI topology generation method has been proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential self balancing and the modulation index of inverters is revealed. Simulation results have verified that the five-level DBFBI topologies have the following advantages:

1. Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density.
2. The series-switch five-level DBFBI has the highest CEC efficiency compared with the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI, and the series-diode five-level DBFBI. Hence, the family of five-level DBFBI topologies is an attractive solution for grid-tied renewable generation systems with high efficiency and high power density.

VI. REFERENCES

[1] X. Guo, R. He, J. Jian, Z. Lu,X. Sun, Z. Lu, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," IEEE Trans. Power Electron., vol. 31, no. 3, pp. 1841–1846, Mar. 2016.

[2] H. Wu, K. Sun, R. Chen, H. Hu, and Y. Xing, " Full-bridge three-port converters with wide input voltage range for renewable power systems," IEEE Trans. Power Electron., vol. 27, no. 9, pp. 3965–3974, Sep. 2012.

[3] X. Wang, F. Blaabjerg, M. Liserre, Z. Chen, J. He, and Y. W. Li, "An active damper for stabilizing power-electronics-based AC systems," IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3318–3329, Jul. 2014.

[4] Y. Gu, Y. Wang, X. Xiang, W. Li, and X. He, "Improved virtual vector control of single-phase inverter for dynamic enhancement based on unified model," IEEE Trans. Energy Convers., vol. 29, no. 3, pp. 611–618, Sep. 2014.

[5] X. Guo, D. Xu, and B. Wu, "Common-mode voltage mitigation for backto- back current-source converter with optimal space-vector modulation," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 688–697, Jan. 2016.

[6] P. Sun, J-S. Lai, H. Qian, W. S. Yu, C. Smith, J. Bates, B. Arnett, A. Litvinov, and S. Leslie, "Efficiency evaluation of a 55 kW soft switching module based inverter for high temperature hybrid electric vehicle drives application," in Proc. 25th IEEE Appl. Power Electron. Conf. Expo., Feb. 2010, pp. 474–479.

[7] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, "Cascade dual buck inverter with phase-shift control," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 2067–2077, Apr. 2012.

[8] P. Sun, C. Liu, J-S. Lai, C-L. Chen, and N. Kees, "Three-phase dualbuck inverter with unified pulse width modulation," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1159–1167, Mar. 2012.

[9] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, "Grid-tie control of cascade dualbuck inverter with wide-range power flow capability for renewable energy applications," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1839–1849, Apr. 2012. .
[10] Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full bridge inverter with hysteresis current control," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3153–3160, Aug. 2009.
[11] Z. Yao and L. Xiao, "Two-switch dual-buck grid-connected inverter with hysteresis current control," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3310–3318, Jul. 2012.
[12] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3118–3128, Sep. 2010.
[13] F. Hong, J. Liu, B. Ji, Y. Zhou, J. Wang, and C. Wang, "Single inductor dual buck full-bridge inverter," IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4869–4877, Aug. 2015.
[14] B. Gu, J. Dominic, J-S. Lai, C-L. Chen, T. LaBella, and B. Chen, "High reliability and efficiency single-phase transformerless inverter for gridconnected photovoltaic systems," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2235–2245, May 2013.
[15] B. Chen, B. Gu, L. Zhang, Z. U. Zahid, J-S. Lai, Z. Liao, and R. Hao, "A high-efficiency MOSFET transformerless inverter for noniolated microinverter applications," IEEE Trans. Power Electron., vol. 30, no. 7, pp. 3610–3622, Jul. 2015.
[16] J-M. Shen, H-L. Jou, J-C. Wu, and K-D. Wu, "Five-level inverter for renewable power generation system," IEEE Trans. Energy Conv., vol. 28, no. 2, pp. 257–266, Jun. 2013.
[17] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
[18] A. Nabae and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
[19] J. Mathew, P. P. Rajeevan, K. Mathew, N. A. Azeezm, and K. Gopakumar, "A multilevel inverter scheme with dodecagonal voltage space vectors based on flying capacitor topology for induction motor drives," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 516–525, Jan. 2013.
[20] J. Rodriguez, J-S. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, control and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Jul. 2002.
[21] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1907–1918, May 2013.