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A Novel Approach in the Design of SRAM using Schmitt-Trigger

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Abstract: We analyze Schmitt-Trigger (ST)-based differen-tial-sensing static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. The proposed ST bitcells incorporate a built-in feedback mechanism, achieving process variation toler-ance-a must for future nano-scaled technology nodes. A detailed comparison of different bitcells under iso-area condition shows that the ST-2 bitcell can operate at lower supply voltages. Mea-surement results on ten test-chips fabricated in 130-nm CMOS technology show that the proposed ST-2 bitcell gives 1.6 higher read static noise margin, 2 x higher write-trip-point and 120-mV lower readmin compared to the iso-area 6T bitcell.

Keywords: Low-voltage SRAM, process tolerance, Schmitt Trigger (ST), Vmin.

I. INTRODUCTION

PORTABLE electronic devices have extremely low power requirement to maximize the battery lifetime. Various device-/circuit-/architectural-level techniques have been imple-mented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order). However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4].

The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write-failure, and access-time failure. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling.

In a given process technology, the maximum supply voltage (referred to as V_{max} for the transistor operation is determined by the process constraints such as gate-oxide reliability limits.$V_{max}$is reducing with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as V_{min}), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, V_{min} is in creasing, and this closes the gap between $V_{max}$and V_{min}. Hence, to enable SRAM bitcell operation across a wide voltage range, V_{min}has to be further lowered. Various design solutions such as read-write assist techniques and bitcell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bitlines, bitcell VSS node, and bitcell VCC node).

In this case, SRAM can be lowered without adding extra transistors to the six–transistor (6T) bitcell. Various bitcelltopologies are also proposed to enable low-voltage operation. Inthis work, we focus only on various bitcell configurations. Webelieve that read-write assist circuits can be applied to these bit-cell configurations for further V_{min}reduction.The remainder of this paper is organized as follows. Section II describes various previously published SRAM bitcells. Section III briefly presents the Schmitt-Trigger (ST)-based SRAM bitcells. Section

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IV shows the detailed V_{min}comparison of various bitcell topologies. Section V presents the measurement results. Section VI summarizes the low-voltage SRAM design discussion.

II. PREVIOUS SRAM BITCELL RESEARCH

Several SRAM bitcells have been proposed having different design goals such as bit density, bitcell area, low voltage op-eration and architectural timing specifications.

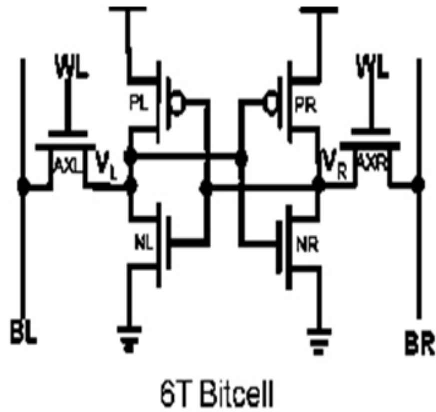


Fig.1: 6Tbitcell

A 6T bitcell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two nMOS access transistors. A single-ended 6T bitcell uses a full transmission gate at one side. Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters.

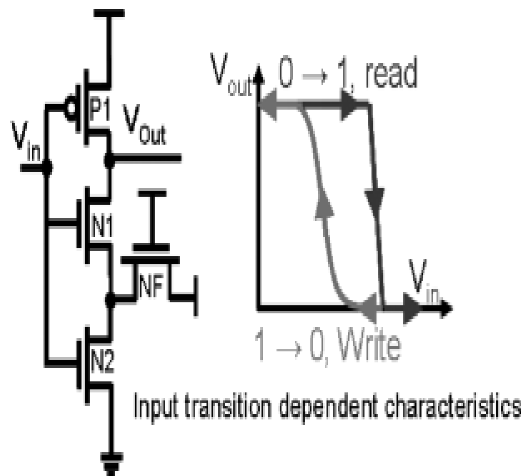


Fig.2.Conceptual ST schematics.

The gate connection of the feedback tran-sistor is connected to the VCC to show the feedback mechanism during 0à1 input transition.

III. SCHMITT TRIGGER SRAM BITCELLS

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in Fig.2. During 0à1 input transition, the feedback transistor (NF) tries to preserve the logic “1” at output (Vout) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated 0à1 by a input transition for the inverter storing logic “1,” higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

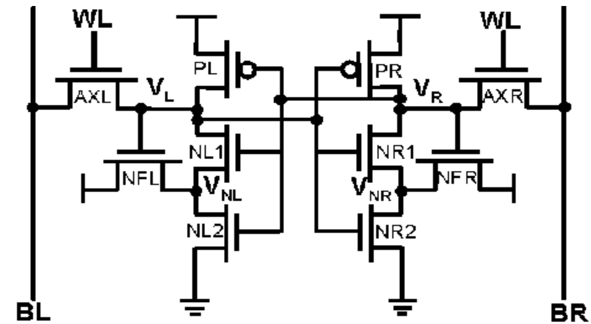
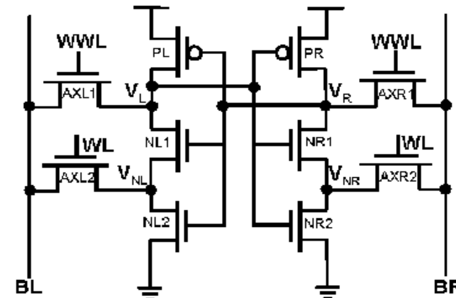


Fig. 3. ST-1 bitcell schematics.



	WL	WWL
Read Mode	1	0
Write Mode	1	1
Hold Mode	0	0

For the 0à1 input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write

operation. Thus, input-depen-dent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell.

A. ST-1 Bitcell

Fig.3 shows the schematics of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-line (WL), and two bitlines (BL/BR). Transistors PL-NL1-NL2-NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the input transition giving the ST action. Detailed operation of the ST-1 bitcell. .**A. ST-1 Bitcell**

ST-2 bitcell schematics

B. ST-2 Bitcell

Fig.ST-2 bitcell schematics shows the schematics of the ST-2 bitcell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bitlines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bitcell, feedback is provided by separate control signal (WL) unlike the ST-1 bitcell, where in feedback is provided by the internal nodes. In the ST-1 bitcell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Detailed operation of the ST-2 bitcell is explained in our earlier work.

IV. SRAM BitcellVminAnalysis

A. Iso-Area Bitcells

1) 6T Iso-Area Bitcell: In this work, we use 6T mincell de-vice widths of 100, 100, and 200 nm for pull-up/access/pull-down transistors, respectively. We can upsize the 6T mincell in various ways. If the bitcell is upsized to be more read-stable, it would affect its write-ability and vice versa. Hence, all transis-tors in the 6T mincell are upsized uniformly to improve the read-stability and write-ability simultaneously.

TABLE I

SUBARRAY AREA ANALYSIS OF 6T/ST BITCELL

	6T Mincell	ST bitecell
Bitecell area	1X	2 X
No. of bitecells	N	N
Total bitcell area	NX	2NX
Array efficiency	70%	70%
Peripheral circuits area	0.43NX	0.86NX
Total sub-array area	1.43NX	2.86NX

B. Read-Failure Probability

Read static noise margin (SNM) is used to quantify the read-stability of the SRAM bitcells. The SNM is estimated graphi-cally as the length of a side of the largest square that can be em-bedded inside the lobes of the butterfly curve . Read-failure probability (P read-fail) is estimated as

P read-fail=Prob.(read SNM<kT).

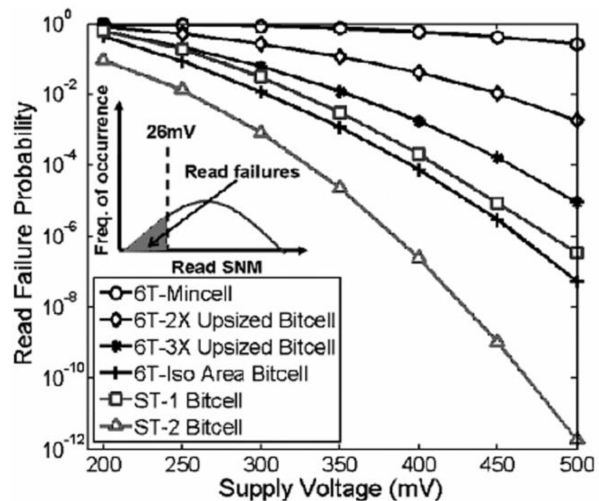


Fig.4. 6T versus ST bitcell: read-failure probability comparison

C. Hold-Failure Probability

Similar to the read stability case, hold-stability is estimated by computing the hold SNM. Fig. 10 shows the hold-failure proba-bility variation versus supply

voltage for 6T and ST bitcells. As shown in inset, hold-failure probability ( ) is estimated as

P read-fail=Prob.(hold SNM<kT).

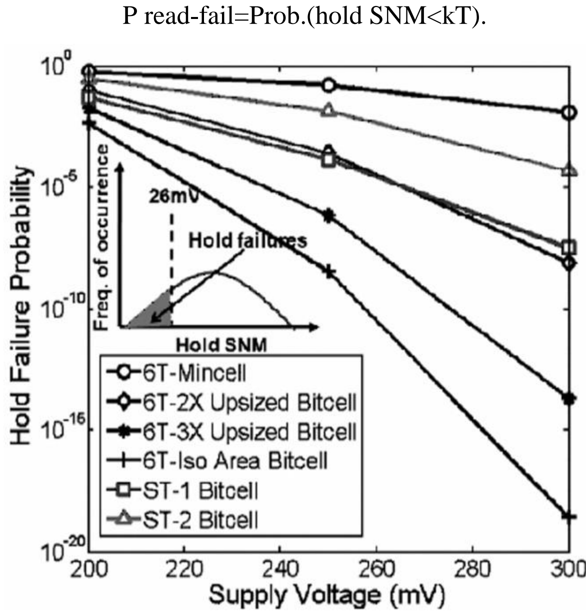


Fig.5. 6T versus ST bitcell: hold-failure probability comparison.

D. Write-Failure Probability

Write-ability of a bitcell gives an indication of how easy or difficult it is to write to the bitcell. Write-trip-point defines the maximum 0-side bitline voltage needed to flip the cell.

The higher the 0-side bitline write-trip-point voltage, the easier it is to write to the cell. Fig. 11 shows the write-failure probability variation versus supply voltage. As shown in inset, write-failure probability is calculated as Pwrite-fail=Prob.(write-trip-point<0mV)

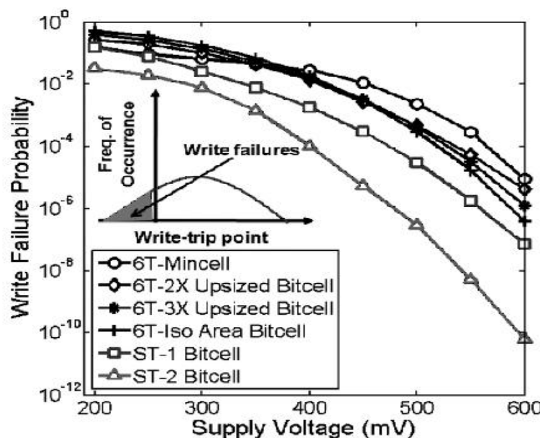
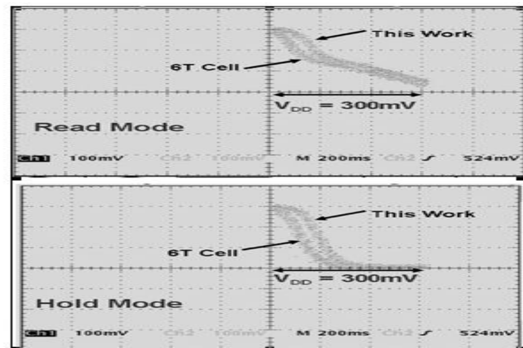


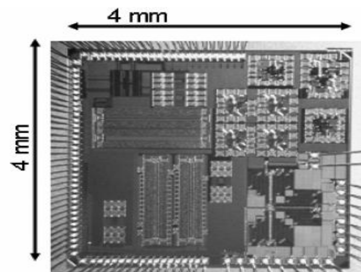
Fig.6. 6T versus ST bitcell: write-failure probability comparison.

V. MEASUREMENT RESULTS

A test-chip with 2Kb SRAM array containing 6T and ST-2 bitcells has been fabricated in 130-nm CMOS technology. For DC measurements, separate isolated 6T/ST-2 bitcells with each transistor having ten fingers were fabricated. Guard rings and dummy fingers (transistors) were implemented for the isolated cell layout in order to minimize the effect of process bias on the finger structures.

The finger structure would result in transistors having threshold voltage same as that of the transistor used in the bitcellarray. Thus, isolated-cell SNM measurement would be equivalent to the actual SRAM array bitcells. In order to characterize the memory failure statistics, built-in self-test circuit was designed. SRAM tester circuit is described in our earlier work [3]. Measurements were done on ten different test-chips to fully characterize both 6T and ST bitcell. Fig. 19 shows the captured voltage transfer characteristics during the read and the hold mode in which the and axes represent the voltages at the storage nodes. This graph clearly shows that





Technology	0.13μm, 8-metal, CMOS
# Transistors	104 K
Silicon area	1.063 mm^2
Read V_{min}	320mV (20Kbits, Room Temp.)
Best case read V_{DD}	150mV (@ 500Hz, Room Temp.)
Frequency	270KHz (V_{DD} = 300mV, $\Delta V_{BL} = V_{DD}/2$)
Leakage current	0.372μA (2Kbits, 300mV, Room Temp.)

Fig.7.Captured read and hold mode characteristicsat 300 mV.

Figures shows the die photograph and the test-chip measurement summary.

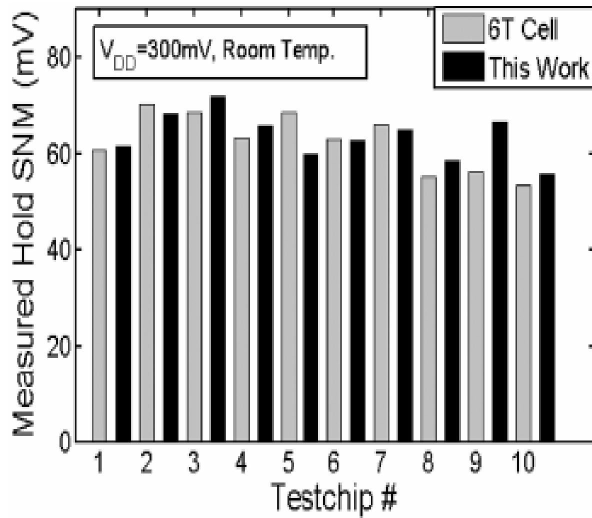


Fig.8: Hold SNM measurement with ten test-chips

Figures shows the possible application space for the proposed ST-2 bitcell. Since the ST bitcells consume 2 x larger area compared with the 6T mincell, at iso-area, the up-sized 6T bitcell has better

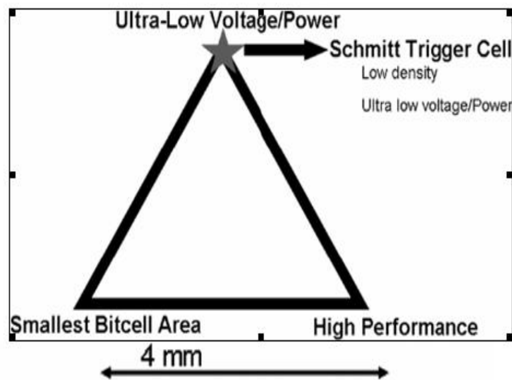


Fig.9.ST SRAM bitcells: application space

performance compared with the ST bitcells (Fig. 15). However, due to built-in process tolerance, the proposed ST bitcells can potentially be useful in applications requiring ultra low voltage. Recently, Wilkerson*et al.* have proposed the use of ST-1 bitcell for tag-arrays to achieve low voltage cache operation .

VI. CONCLUSION

Lowering the supply voltage is an effective way to achieve ultra-low-power operation. In this work, we evaluated ST-based SRAM bitcells suitable for ultra-low-voltage applications. The built-in feedback mechanism in the proposed ST bitcell can be effective for process-tolerant, low-voltage SRAM operation in future nanoscaled technologies. Monte Carlo simulations in 65-nm technology predict lower for the proposed ST-2 bitcell under the iso-area condition. Measurement results with a 130-nm test-chip clearly demonstrate the effectiveness of the proposed ST-2 bitcell for successful ultralow-voltage operation.

A. Future Work

In this paper, 6T/8T/10T/ST SRAM bitcell topologies are an-alyzed for achieving low voltage operation. ST bitcells offer low voltage operation with 2 area overhead. On the other hand, various read/write assist techniques achieve significant reduction, with lower area overhead. Hence, for a given constraint, optimal combination of the bitcell topology read/write assist technique should be chosen for minimal area/power overhead. Thus, the effectiveness of read/write as-sist techniques for each of the bitcell topology needs to be in-vestigated for achieving lower.

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VII. REFERENCES

[1] K. Roy and S. Prasad, Low Power CMOS VLSI Circuit Design, 1st ed. New York: Wiley, 2000.

[2] N. Yoshinobu, H. Masahi, K. Takayuki, and K. Itoh, “Review and future prospects of low-voltage RAM circuits,” IBM J. Res. Devel., vol. 47, no. 5/6, pp. 525–552, 2003.

[3] A. Bhavnagarwala, X. Tang, and J. Meindl, “The impact of intrinsic device fluctuations on CMOS SRAM cell stability,” IEEEJ. Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[4] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, “Modeling of failureprobability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS,” IEEE Trans. Comput.-Aided Design (CAD) Integr. Circuits Syst., vol. 24, no. 12, pp. 1859–1880, Dec. 2005.

[5] M. M. Khellah, A. Keshavarzi, D. Somasekhar, T. Karnik, and V. De, “Read and write circuit assist techniques for improving of dense 6T SRAM cell,” in Proc. Int. Conf. Integr. Circuit Design Technol., Jun. 2008, pp. 185–189.