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Implementing A GDI Technique Based Optimized Low Power 2-Bit Magnitude Comparator

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Abstract: As technology scales into the nanometer regime leakage current, active power, delay and area are becoming important metric for the analysis and design of complex circuits. The main concern in mobile and battery based systems are area and power dissipation. In order to reduce area and power dissipation two bit magnitude comparator using GDI (Gate Diffusion Input) technique is designed in this project. This two bit magnitude comparator using GDI technique is considered to achieve less area, reduced power and high speed performance. In this paper initially two bit magnitude comparator is designed with and without GDI technique which is simulated and synthesized using Cadence Virtuoso tool. The two bit GDI based magnitude comparator is designed with the help of full adder which is the basic building block of ALU. The simulation and synthesis of two bit magnitude comparator is performed by using cadence IUS (Incisive unified simulator) tool. The power and timing analysis of two bit magnitude comparator is performed using cadence RTL compiler. By using cadence encounter tool, the two bit magnitude comparator is implemented on SoC.

Keywords: Magnitude Comparator, GDI (Gate Diffusion Input) Technique, Full Adder, Cadence IUS (Incisive Unified Simulator) Tool.

I. INTRODUCTION

In the last twenty years or so by far, the strongest growth area of the semiconductor industry has been in silicon Very – Large Scale Integration (VLSI) technology. The sustained growth in VLSI technology is fuelled by the continued shrinking of transistors to ever smaller dimensions. The benefits of miniaturization are higher packing densities, higher circuit speeds, and lower power dissipation have been key in the evolutionary progress leading today's computers and communication systems that offer superior performance, dramatically reduced cost per function, and much reduced physical size, in comparison with their predecessors. VLSI circuits have found a lot of applications in the recent development of ICs. The dimensions of transistors have shrunk enormously, which has a great positive impact on VLSI technology. The evolution of VLSI device technology from the invention of first bipolar transistor, MOSFET, CMOS up to the VLSI era, the power dissipation aspects of various types of transistor technology is always a researcher's interest. At the circuit level, considerable potential for power saving exist by the proper choice of logic style for implementing combinational circuits.

The various methodologies and topologies to achieve the required function such as conventional CMOS, nMOS Pass transistor logic and transmission gates can reduce layout area and consequently power dissipation. nMOS Pass transistor logic technique is better than the conventional CMOS technique in high speed and low power logic circuit design because of reduced number of transistors. However, the major drawback of nMOS Pass transistor logic technique is the reduced drive current and hence slower speed of operation at the reduced supply voltage. A new logic style first proposed by A. Morgenshtein, GDI technique is superior over other design techniques in terms of low power and high speed VLSI design as this technique uses a simple GDI cell consisting of only two transistors, to implement various complex logic functions. This technique improves the logic level swing, characteristic performances and also allows a simple design of any logic circuit using a small GDI cell. GDI technique enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with conventional CMOS, nMOS Pass transistor logic and transmission gates. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit.

Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance. The simulations are carried out for power, Delay, Power Delay Product at varying supply voltages from 1.0v to 2.0v. Simulations are performed at 180nm technology in Tanner EDA Tool. In this paper, GDI Magnitude Comparator is proposed which has an advantage of minimum power dissipation, less number of

transistors required as compare to conventional CMOS magnitude comparator. The rest of this paper is organized as follows. Section II discusses about literature survey of the paper. Section III discusses implementation of two bit magnitude comparator using GDI technique circuit. Section IV shows the simulation results. Finally, section V concludes this work.

II. LITERATURE SURVEY

A.CMOS Magnitude Comparator

Now a day's CMOS (Complementary Metal Oxide Semiconductor) logic style is the primary technology in the Semiconductor Industry. Conventional method is used to construct schematic of 2-Bit magnitude comparator using CMOS technique. Here is the brief description of CMOS inverter. Fig. 1 show symbol of CMOS inverter consists of pMOS and nMOS transistor connected at the drain and gate terminal, a supply voltage V DD at the pMOS source terminal and GND connected at the nMOS source terminal. Whereas input (A) is connected to the gate terminals and output (Abar) is connected to the drain terminal. If input A=O, then pMOS is ON and provide low impedance path from VDD to output (Abar). At that time nMOS is in OFF condition, thus output (A bar) approach to high level that is VDD.

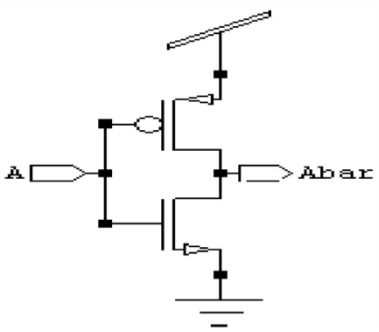

Fig.1. CMOS inverter.

If input A= l, then nMOS is ON and pMOS is in OFF condition, nMOS provide low impedance path from output (Abar) to ground. Therefore, output (Abar) approach to low level that is OV. The substrate pMOS is always connected to VDD and nMOS substrate is always connected to GND. The CMOS inverter provides two important advantages, low static power dissipation and high noise margin. It is also balanced device, so it is called ratio less device. An N-Bit magnitude comparator is shown in Fig. 2, it compares two n bit binary number A and B and the outcome of n bit magnitude comparator is denoted by A< B (FI), A= B (F2), A> B (F3).

Fig. 2. N-bit magnitude comparator.

To determine whether A is greater than B or vice versa and then firstly check the most significant bit If most significant bit of both inputs is different, e.g. suppose most significant of A is 1 and most significant bit of B is 0 then A> B, if condition is reverse then A <8. If most significant bit of both the input is equal then go for next bit and then compare the next bit of both the input If both the inputs are same then A= B. The outcome of 2-Bit magnitude comparator is shown in Table 1 for different combination of input According to different condition of input, the equations are as follows:

$$A> B: = A1\ B1 + AO\ BO(A1\ B1 + A1B1):= A1\ B1 + AO\ BO(X1) \quad (1)$$

$$A = B:= (A1\ B1 + A1\ B1)(AO\ BO + AOBO):= Xl\ XO \quad (2)$$

$$A < B:= A1B1 + AOBO(A1\ B1 + A1B1) := AIBI + AOBO(Xl) \quad (3)$$

TABLE I: Truth Table of 2-bit Magnitude Comparator

A1	A0	B1	B0	F2	F1	F3
o	o	o	o	1	o	o
o	o	o	1	o	1	o
o	o	1	o	o	1	o
o	o	1	1	o	1	o
o	1	o	o	o	o	1
o	1	o	1	1	o	o
o	1	1	o	o	1	o
o	1	1	1	o	1	o
1	o	o	o	o	o	1
1	o	o	1	o	o	1
1	o	1	o	1	o	o
1	o	1	1	o	1	o
1	1	o	o	o	o	1
1	1	o	1	o	o	1
1	1	1	o	o	o	1
1	1	1	1	1	o	o

According to this condition, 2-Bit conventional CMOS magnitude comparator schematic is made as shown in Fig. 3. Looking into Fig3, it reveals that 2-Bit Magnitude Comparator requires large number of transistors i.e.; 66. This large transistor count consumes more power and larger area, so to overcome this problem GDI technique is used to construct magnitude comparator.

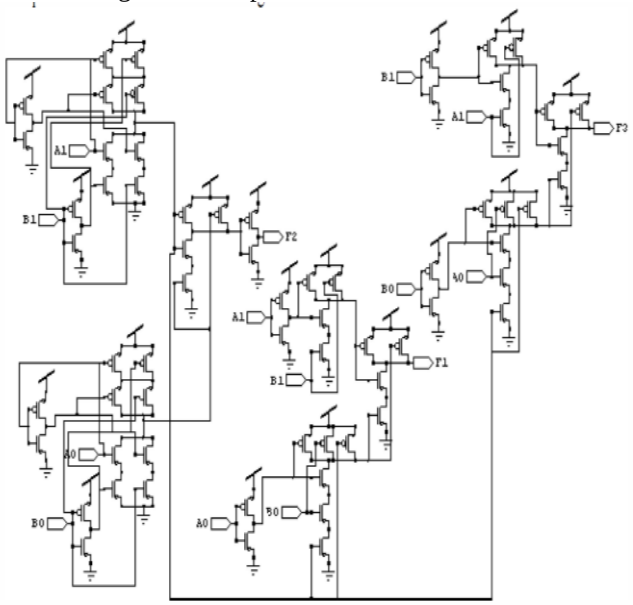

Fig.3. Schematic of 2- Bit Magnitude Comparator using Conventional CMOS Logic Style.

B. SoC Technology

A system on a chip or system on chip (SoC or SOC) is an integrated circuit (IC) [4] that integrates all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions all on a single chip substrate. SoCs are very common in the mobile electronics market because of their low power consumption. A typical application is in the area of embedded systems. The contrast with a micro-controller is one of degree. Microcontrollers typically have under 100 kB of RAM (often just a few kilobytes) and often really single-chip-systems, whereas the term SoC is typically used for more powerful processors, capable of running software such as desktop versions of Windows and Linux, which need external memory chips (flash, RAM) to be useful, and which are used with various external peripherals. In short, for larger systems, the term system on a chip is a hyperbole, indicating technical direction more than reality increasing chip integration to reduce manufacturing costs and to enable smaller systems. When it is not feasible to construct SoC for a particular application, an alternative is a system in package (Sip) comprising a number of chips in a single package. In large volumes, SoC is believed to be more cost effective than Sip since it increases the yield of the fabrication and because its packaging is simpler.

Another option, as seen for example in higher end cell phones and on the Beagle Board, is package on package stacking during board assembly. The SoC chip includes processors and numerous digital peripherals, and comes in ball grid package with lower and upper connections. The lower balls connect to the board and various peripherals, with the upper balls in a ring holding the memory buses used to access NAND flash and DDR2 RAM. Memory packages could come from multiple vendors. A SoC consists of both the hardware described above, and the software controlling the microcontroller, microprocessor or DSP cores, peripherals and interfaces. The design flow for SoC aims to develop hardware and software in parallel. Most SoCs are developed from prequalified hardware blocks for the hardware elements described above, together with the software drivers that control their operation. Of particular importance are the protocol stacks that drive industry standard interfaces like USB. The hardware blocks are put together using CAD tools, the software modules are integrated using a software development environment. Chips are verified for logical correctness before being sent to foundry. This process is called functional verification and it accounts for a significant portion of the time and energy expended in the chip design life cycle (although the often quoted figure of 70% is probably an exaggeration).With the growing complexity of chips, hardware verification languages like System Verilog, System C, e, and Open Vera are being used. Bugs found in the verification stage are reported to the designer.

III. PROPOSED METHODOLOGY

A. Magnitude Comparator using GDI Technique

The logic diagram of 2-Bit Magnitude Comparator based on full adder is shown in Fig. 4. A basic full adder has three inputs and two outputs. In full adder logic sum output is useful to get output F2 and Cout is useful to get output Fl. As shown in Fig. 4, require XOR gate, MUX & AND gate for logic circuit of full adder which useful to design magnitude comparator, For the logic sum require XOR gate and for carry output (Cout) require AND & OR gate. XOR gate IS basic building block of full adder; many refinements have been done to reduce the number of transistor and also for better performance of XOR gate.

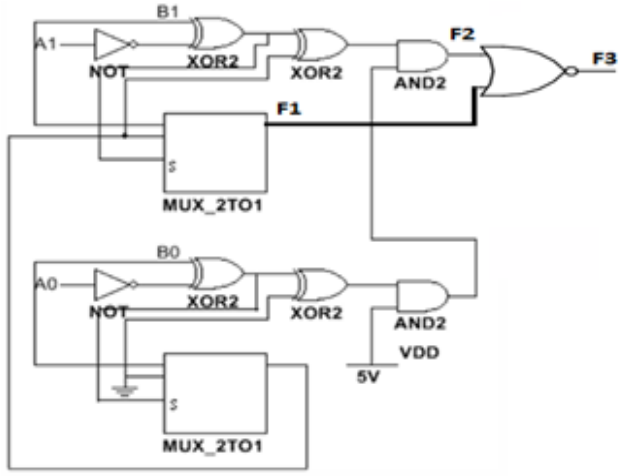

Fig.4. Logic diagram of 2-bit magnitude comparator using full adder.

As discussed, GDI technique require less transistor for AND, OR and XOR gate in compare conventional CMOS logic technique. So GDI technique is preferred to construct this logic function in compare to CMOS logic style. If one inverted input is given to XOR gate then it act like XNOR gate, so reduce the number of transistor XOR gate with inverter input is replace with XNOR gate. GDI technique is used to construct 2-Bit magnitude comparator based on full adder is shown in the Fig. 5. For the output of F3, the condition used is, if F2 and Fl is 0 then F3 is I. GDI technique magnitude comparator requires (30 transistor) less no of transistor in compare to conventional CMOS magnitude comparator (66 transistor).

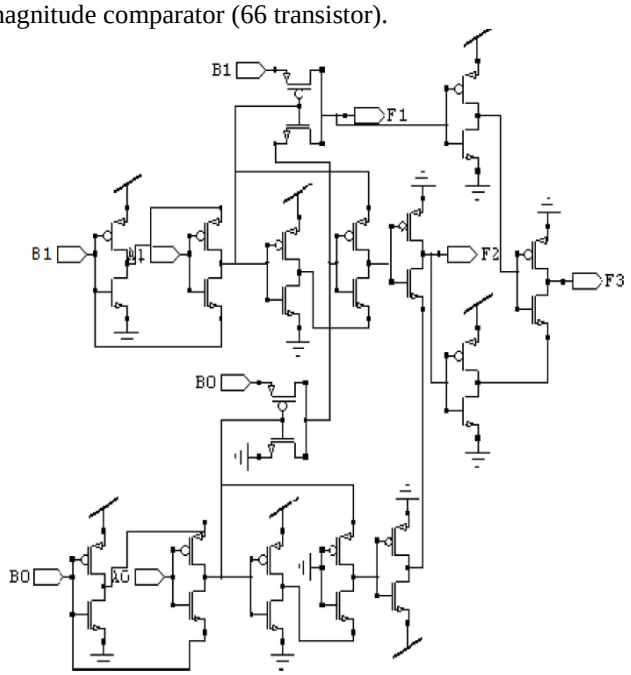

Fig.5. Schematic of 2-bit magnitude comparator using GDI Technique.

Based on CMOS 180nm process technology, the proposed comparator is proven to have the minimum power consumption and less area by Cadence simulation comparing with conventional CMOS logic. Due to the minimum power consumption and less area, the comparator us greatly improves the overall performance.

B. Power Calculation

Power analysis is an estimation of power dissipation, both dynamic and static, of the chip in various operating modes. Static power analysis is the calculation of leakage power. Static power dissipated is power dissipated during steady state condition. A cell dissipates leakage power when voltage is applied even if it is not switching. As the process geometry shrinks, leakage power is becoming a greater percentage of a chip's overall power dissipation. It is something that we cannot ignore. Dynamic power consists of power dissipated inside a cell (mostly due to short-circuit current during switching) and power dissipated to charge/discharge net capacitance. Dynamic power dissipation is power dissipated during transient state condition. Dynamic power is a function of voltage, toggle rate, and net loading.

TABLE II: Comparison between CMOS Logic and GDI Technique in 2 Bit Magnitude Comparator

S . N O	Number of transistors	Power Consumption	Leakage Power
CMOS logic	6 6	1.20075272 uw	0.002109552 uw
GDI technique	3 0	0.7063251260 uw	0.0012409130 uw

IV. SIMULATION RESULTS

Simulation results are implemented in cadence 180nm technology with statement of the problem and the analysis, simulation and synthesis are done in cadence virtuoso, IUS as shown in Figs.6 to 9.

A. Waveform of 2-Bit Magnitude Comparator Using Conventional CMOS Logic

Fig.6. 2-bit magnitude comparator using conventional.

B. CMOS Logic Simulation In Cadence

In this waveform the first 4 are inputs A0, A1, B0, B1 with 1.2 volts and last 3 are outputs F1, F2, F3. X-axis is time period in nanoseconds and Y-axis is voltage in volts. This is the waveform of 2-bit magnitude comparator using conventional CMOS logic simulation.

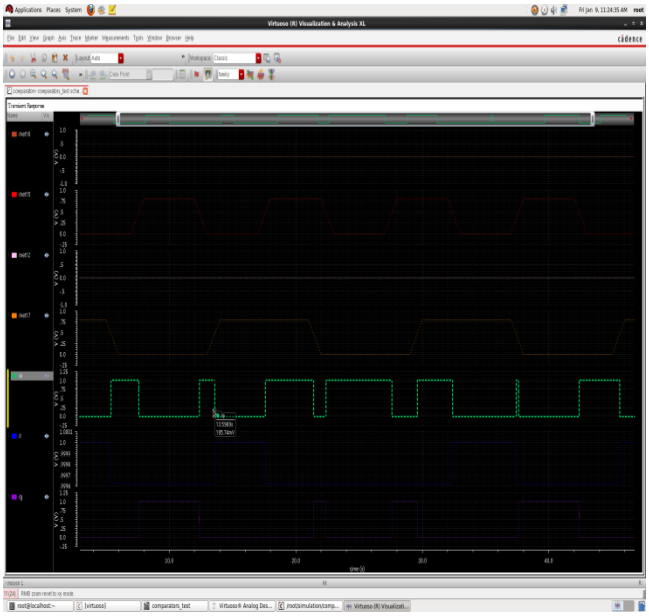

Fig.7. Waveform of 2-bit magnitude comparator using GDI technique simulation.

In this waveform the first 4 waveforms are inputs A0, A1, B0, B1 with 1.2volts and last 3 waveforms are outputs F1, F2, F3. X-axis is time period in Nano seconds and Y-axis is voltage in volts. This is the waveform of 2-bit magnitude comparator using GDI technique simulation.

C. SoC Results of 2 Bit Magnitude Comparator

Fig8 shows the chip design of 2-bit magnitude comparator in SoC Encounter.

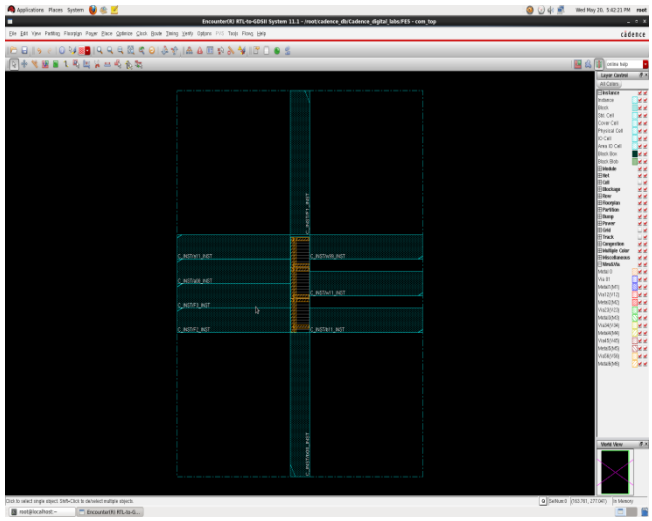

Fig.8.Chip design layout of 2-bit magnitude comparator in SoC.

The fig 8 is the layout of chip design of 2-bit magnitude comparator is implemented in cadence SoC Encounter. After getting the results in cadence virtuoso, IUS and RTL compiler the chip design is done in SoC encounter by creating LEF file for 2-bit magnitude comparator using GDI technique circuit in virtuoso and netlist for designed 2-bit magnitude comparator in RTL compiler. The ALU chip design for SOC is achieved by combining LEF file and netlist in cadence SOC encounter tool.

D. Simulation Results of 2-Bit Magnitude Comparator Using Full Adder

Implemented the 2-bit magnitude comparator using full adder program in IUS obtained the design of 2-bit magnitude comparator using full adder in cadence IUS (incisive unified simulator).

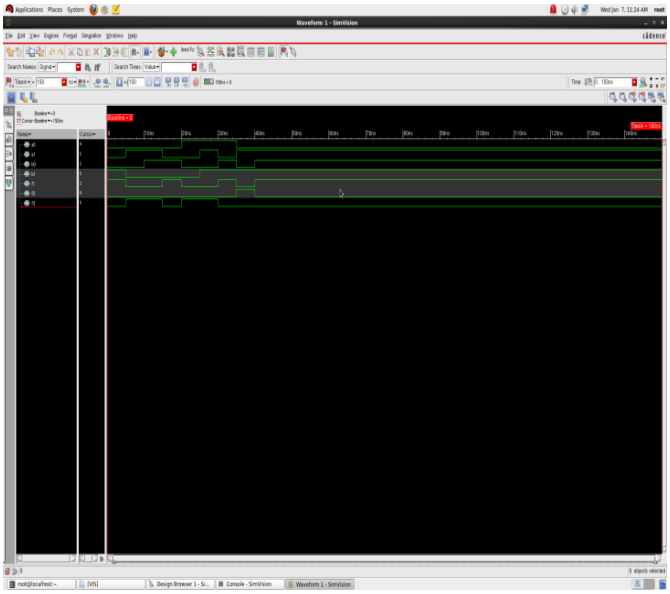

Fig.9.Output waveform of 2-bit magnitude comparator using full adder waveform.

This is the waveform of 2-bit magnitude comparator using full adder with A0, A1, B0, B1 as inputs and F1, F2, F3 as outputs.

V. CONCLUSION

The performance of the proposed two bit magnitude comparator using GDI technique with the help of full adder logic has shown good performance in compare to existing conventional CMOS based design. The comparative performance of conventional CMOS and proposed GDI magnitude comparator implemented in SoC, ISE, Virtuoso and Cadence RTL Encounter with respect to power consumption at different range of input voltage has been discussed in above section. The smaller area of proposed two bit GDI magnitude comparator results into shorter interconnects and thus less cross talk., enable more efficient placement and routing. Thus, it is concluded that proposed two bit magnitude comparator based on GDI technique require less power and smaller area in comparison to CMOS magnitude comparator. Hence, this new design is good option for low power efficient system design.

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