



Closed Loop Control of Switching Pattern Selection scheme Based Cascaded Multilevel Inverter Fed Three-Phase Grid

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Abstract: The objective of this paper focus on closed loop control of switching pattern selection scheme based cascaded multilevel inverter fed three-phase grid. It gives several advantages compared to the typical 3-phase bridge inverter in terms of lower dv/dt stresses, lower electromagnetic compatibility, smaller rating and better output features. The proposed method has been designed an eleven-level cascaded multilevel inverter by using sinusoidal pulse width modulation technique. The selected pattern has been exposed to give superior performance in load voltage, total harmonics distortion and capacitor voltage fluctuation. The performance of proposed strategies is confirmed through simulation investigations.

Keywords: Cascaded Multilevel Inverter, Total Harmonic Distortion (THD), Sinusoidal pulse width modulation (SPWM)..

I. INTRODUCTION

Cascade multilevel inverter is a power electronic device built to synthesize a desired ac voltage from several levels of dc voltages. Such inverters have been received increasing attention in the past few years for high power application. A small total harmonic distortion is the most important feature of these inverters. Basically cascade multilevel inverter is used in this work with proposed control circuit to control the output voltage using sinusoidal pulse width modulation (SPWM). The requirement of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters due to high efficiency with low switching frequency control method. The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the AC side can take several discrete levels of equal magnitude.

The Harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two-level voltage waveform. The cascaded H-bridge apart from other multi-level inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency inverters. An alternate method of cascading inverters involves series connection of two, three-phase inverters through the neutral point of the load. Past research has shown this concept for cascading two-level inverters and multi-level inverters. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter

systems can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices.

Multilevel power inverters employ power semiconductor switches in the inverter to select one or more of multiple dc voltage sources to create staircase voltage waveform at the inverter output. Capacitors batteries or renewable energy voltage sources can be used as a DC voltage sources. The control of the power switches permits the addition of the multiple DC sources in order to achieve desired staircase waveform at the high power output. This scheme does not require any modification in the carrier or modulating signal. The modeling of in this paper highlights significance of an eleven level cascaded multilevel inverter.

II. CASCADED MULTILEVEL INVERTERS

A. Basic structure and operating principle

The multilevel inverters have gained considerable attention over the past decade for high-voltage and power applications in industries. The primary advantage of multilevel inverters is their smaller output voltage step, which results in high power quality, lower harmonic components, better electromagnetic compatibility and lower switching losses. An eleven – level cascaded multilevel inverter configuration is shown in Figure1. Each SDCS is associated with a single-phase full-bridge Inverter. The DC terminal voltages of different level inverters are connected in series, different combination of the four switches, S_1 - S_4 , each inverter level can generate three different voltage outputs, +Vdc, -Vdc, and zero.

The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where 's' is the number of DC sources. The proposed method has been designed an eleven - level cascaded multilevel inverter, which has five single-phase full-bridge inverter connected in series, it has produce the desired eleven-level phase voltage. Phase voltage waveform for an eleven - level cascaded multilevel inverter with five SDCSs and five full bridges is shown in Figure 1.

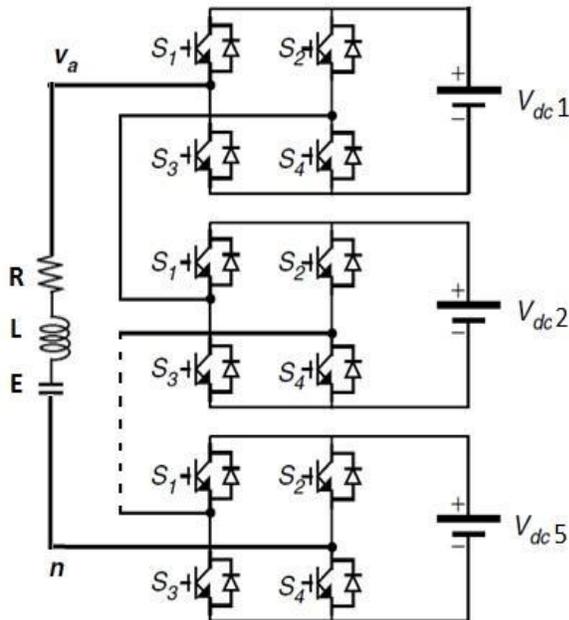


Figure1. Cascaded Multilevel Inverter

The phase voltage is given by

$$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5}$$

The Fourier Transform for this waveform follows

$$V(\omega t) = \sum 4V_{dc}/\pi n [\cos(n\theta 1) + \cos(n\theta 2) + \dots + \cos(n\theta s)] \times \sin(n\omega t)/n,$$

Where $n = 1, 3, 5, 7, \dots$

The magnitudes of the Fourier coefficients normalized with respect to V_{dc} are as follows

$$H(n) = 4/\pi n [\cos(n\theta 1) + \cos(n\theta 2) + \dots + \cos(n\theta s)] \times \sin(n\omega t)/n,$$

Where $n = 1, 3, 5, 7, \dots$

B. Modulation Scheme

The control technique of sinusoidal pulse width modulation (SPWM) strategy is employed. In this method, a number of triangular waveforms are compared with a controlled sinusoidal modulating signal. The switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal. The proposed eleven - level inverter, one modulating signal and ten carrier waves are necessary for each phase of the inverter as shown in Figure 2.

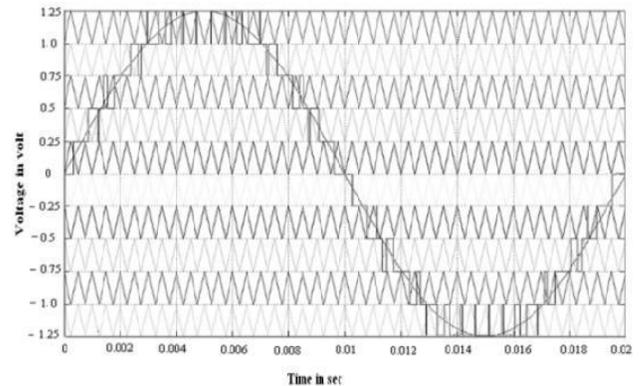


Figure2. Modulation Scheme of Eleven-Level

The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from +1.25V to -1.25V. The amplitudes of the ten carriers waves vary in the step of +0.25V. In the positive half cycle the comparator output will have the value high, if the amplitude of the modulating signal is greater than that of the carrier wave and zero otherwise. Similarly for the negative half cycle, if the modulating signal is lower than the carrier wave, the output of the comparator is high and zero otherwise.

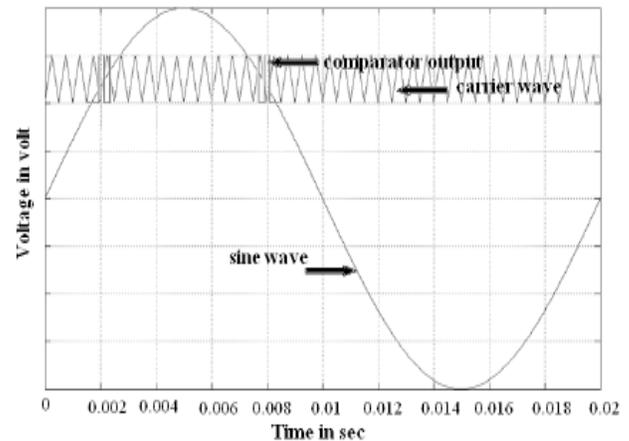


Figure3. Sinusoidal and Carrier wave comparison

In the Eleven-level cascaded multilevel inverter each carrier waveform and sine waveform are compared individually. The switching pulses generation technique of the power semiconductor device is shown in figure 2. The each comparator output is given to cascaded multilevel inverter switching devices. The simulation model of switching pulse generation is shown in figure 3. The comparator output is directly given to S1 and S4 as shown in figure 3. In the eleven-level cascaded multilevel inverter ten carrier waveforms and a sine waveforms are compared with individual comparator. This comparator output is given to S_j where $j=1$ to 10, by using this manner inverter obtained eleven levels phase voltage.

III. SIMULATION MODEL AND RESULTS

A. Simulation Model

Three phase MATLAB/ SIMULINK simulation model of cascaded multilevel inverter is shown figure 4.

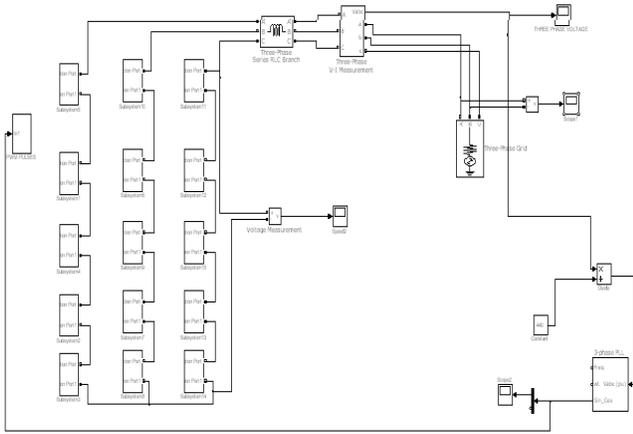


Figure4. Simulation Model

B. Simulation Results

The eleven-level cascaded multilevel inverter has been simulated using MATLAB; the inverter is supplying a balanced three-phase voltage to three-phase grid. The cascaded multilevel inverter balanced output three phase voltage is 400V, 50Hz. The eleven-level inverter devices have been assumed to be nearly ideal for simulation. Inverter output quantities such that output of inverter phase voltages, line voltages and three phase balanced line voltage are shown in Figure 5, figure 6 and figure 7 respectively. Three phase voltages are clearly in correct phase relation and have eleven-levels ($V_{dc}/2, 2/5V_{dc}, 3/10 V_{dc}, V_{dc}/5$ and $V_{dc}/10, 0, -V_{dc}/2, -2/5V_{dc}, -3/10V_{dc}, -V_{dc}/5$ and $-V_{dc}/10$).

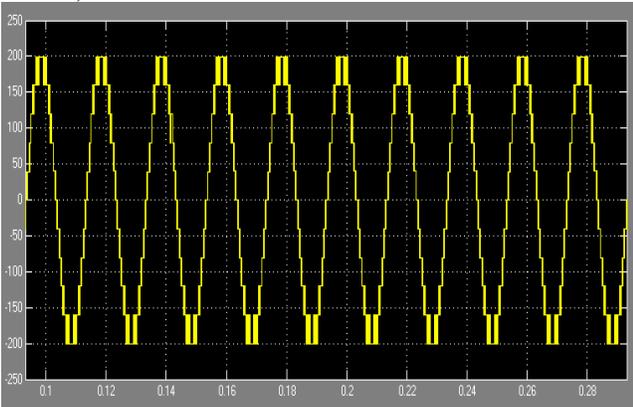


Figure5. Phase Voltage of Cascaded Multilevel Inverter

Table 1. Comparison of THD

Five-level (% of THD)	Seven Level(% of THD)	Nine-level (% of THD)	Eleven-level (% of THD)
26.26	17.76	13.22	10.62

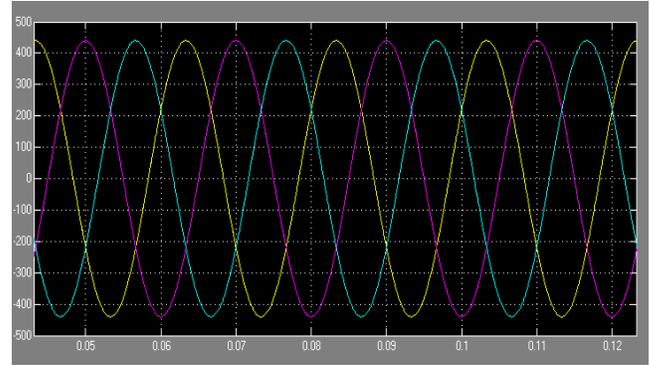


Figure6. Three phase line voltage cascaded MLI

Cascaded multilevel inverter output is fed to the three-phase grid to verify the basic performance of the inverters like voltage fluctuation, frequency variation, etc. Since the three-phase grid is treated as the load to the multilevel inverter, any variation in the performance of multilevel inverter reflects on the performance of grid. The proposed method of an eleven -level cascaded multilevel inverter fed to three-phase grid performance is verified through simulation investigations.

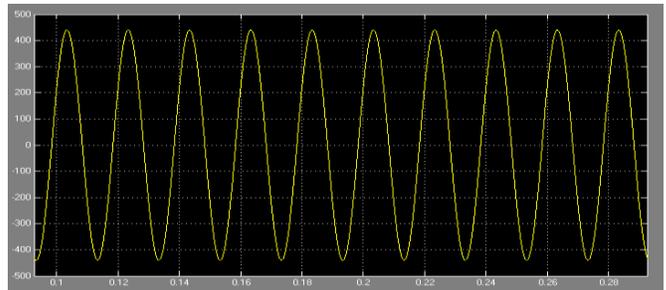


Figure7. Line Voltage of Three-Phase Grid

Total Harmonic Distribution of eleven-level cascaded multilevel inverter has 10.62% it illustrated in figure 10. The eleven-level cascaded multilevel inverter THD values are reduced compared to THD of seven -level and nine level cascaded multilevel inverter. The THD value of seven and nine are 17.76%, 13.34% respectively as shown table I.

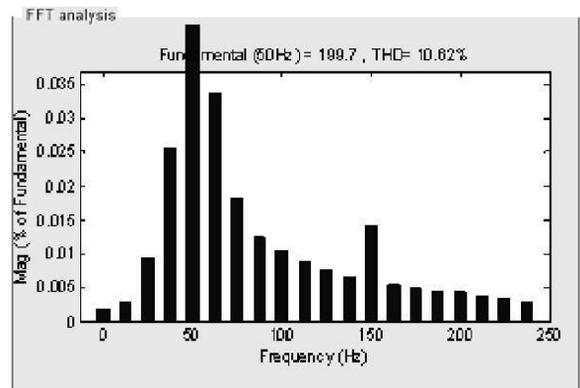


Figure10. THD of Eleven-Level Cascaded Multilevel Inverter

IV.CONCLUSION

In this paper, the basic structure and operating characteristics of cascaded multilevel inverter have been described by taking an eleven-level inverter configuration. The eleven-level cascaded multilevel inverter has been illustrating in simulation results by using MATLAB. The inverter cell is low means the design of the inverter switch pattern is easiest. Multilevel inverter is to obtain a high resolution. The technique is used to improve the level of the inverter and extends the design flexibility and reduces the harmonics.

V. REFERENCES

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