Analysis of Routing Algorithm for 3D NoC Architecture

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**Abstract:** Network on Chip (NoC) is the most promising on-chip communication architecture. The three dimensional integration of NoC is achieved by stacking 2D layers. This work proposed a deterministic routing scheme for choosing the 3D node with mesh topologies. In this architecture, the emerging 3D VLSI integration and process technologies allow the new design opportunities in 3D Network-on-Chip. The 3D NoC can reduce significant amount of wire length for local and global interconnects. The arrangement of 3D integration offers opportunities for new circuit architecture. The unique feature of this model is the search for the proximal vertical 3D node towards the destination router. Depending on the traffic around the routed node the proposed routing algorithm provides paths for routing packets. This paper work on routing algorithm which is based on geometrical arrangement for 3D network on chip (NoC) architecture. This proposed algorithm partitions the geometrical space into quadrants and selects the nearest wrap-around edge to connect the destination node. Thus, the presented algorithm guarantees minimal paths to each destination based on routing regulations and avoid congestions and also has constant node degree, recursive structure, simple communication algorithms, and good scalability.

**Keywords:** 3D IC’s, 3D Noc, Mesh Topology, XYZ Routing Algorithm.

I. INTRODUCTION

With shrinking geometries, global interconnects became the principal performance bottleneck for superior Systems-on-Chip (SoCs) \cite{1}, \cite{2}, \cite{3}. These long interconnects are quickly turning into a performance impediment in terms of communication latency and power \cite{4}. The Network-on-Chip (NoC) model is rising as a revolutionary methodology to seek out the performance limitations arising out of long interconnects, outperforming variant thought bus architectures \cite{5},\cite{6}. Additionally to providing an answer for the global wire delay disadvantage, the NOC paradigm additionally eases integration of high numbers of property (IP) cores during a very single SoC. However, restricted floor-planning selections of the 2D integrated circuits (ICs) limit the performance enhancements arising out of NOC architectures. As shown in Fig. 1, 3D ICs, that contain multiple layers of active devices, have the potential for enhancing system performance \cite{7}, \cite{8}, \cite{9}, \cite{10}. to keep with \cite{7}, 3D ICs yield performance enhancements even at intervals the absence of scaling. Typically this can be usually often the results of the reduction in interconnect length. Besides this clear profit, package density is raised considerably, power is reduced from shorter wires, and circuitry could also be lots of proof against noise \cite{7}. The performance improvement arising from the benefits of NoCs area unit reaching to be considerably enlarge if 3D ICs are adopted as a results of the elemental fabrication methodology. The blending of 2 rising paradigms, NOC and 3D IC, permits for the creation of latest structures that modify necessary performance enhancements over lots of ancient solutions. On the opposite hand, Network-on-chip suffers from the delay and high power consumption of long wires and additionally the expansion of hop-count once the amount of IP cores grows. Utilization of the dimension (3D technology) can lead to a serious reduction in power and average hop-count in Networks-on-Chip (NoC) \cite{39}. The mixture of 3D technology and intelligence officer approach ends in denser integration fully totally different on-chip layers with different technologies like on-chip memory SoCs. In addition, TSV technology, as a result of the foremost promising technology in 3D integration, offers short and fast vertical links inhumed stacked layers \cite{28}. Therefore, Vertically-Partially-Connected 3D-NoC has been introduced to target 3 dimensional (3D) technology and high yield. Moreover, Vertically-Partially-Connected 3D-NoC is flexible, as a result of the particular incontrovertible fact that the quantity, placement, and assignment of the vertical links in each layer could also be determined based upon the requirements of the design. However, there area unit challenges to gift a potential and superior Vertically-horizontally-Connected 3DNoC attributable to the removed vertical links between the layers.

II. RELATED WORK

As the presented work addresses inter-layer pairing, adaptive routing and observation problems with 3D NoCBus Hybrid mesh architectures, the discussion of connected work has centred on 3D Networks-on-Chip architectures and system observation and management techniques. Three
Dimensional integrated circuits evolved to deal with the constraints of interconnect scaling by stacking active semiconductor layers. A close description of the challenges faced to manufacture the 3D ICs is provided in [4]. The authors have shown that 3D ICs area unit power and performance economical, however once the 3D NOC is taken under thought, the statistics are quite completely different. The 3D NOCs are extension to the 2D NoC design. For each NOC router of topology, two further ports are required ensuing a 7×7 crossbars rather than 5×5 crossbar for the second mesh design. Since crossbar power will increase quadratically with the amount of ports the power consumption for a 3D router is far higher than for a 2D router [9]. The solution to the facility consumption for a 3D router has been projected by Li et al. [10]. The projected architecture is stacked mesh design. Due to one hop vertical communication and 6×6 routers, proposed architecture is economical enough in terms of power consumption and latency. Since the bus may be a shared medium it doesn't enable coincident communication within the third dimension, but it's been shown that the Ddma bus out performs associate NOC for the vertical communication as long because the variety of second planes is a smaller amount than 9. Thus, bus medium offers an enough degree of quantifiability for the dimension. The difficulty with this design is that every packet is traversed through 2 buffers: the supply output buffer and destination input buffer as we'll discuss later, the output buffer hinders implementing congestion-aware layer communications. We tend to improve the design to further enhance the throughput by using the accessible communication resources.

In [9], 3D ICs were projected to enhance performance of chip multiprocessors. Drawing upon 3D IC analysis, they chose a union of buses and networks to supply the interconnect material between CPUs and L2 caches. The performance of this fusion of intelligence agent and bus architectures was evaluated exploitation customary processor benchmarks. However, this analysis pertains solely to chip multiprocessors and does not think about the utilization of 3D network structures for application-specific SoCs (see fig 2). Three-dimensional NoCs are analysed in terms of temperature in [11]. Pavlidis and Friedman [13] compared second MESH structures with their 3D counterparts by analysing the zero-load latency and power consumption of every network. This is often associate degree analysis that shows a number of the benefits of 3D NoCs, however it neither applies any real path nor will it live different relevant performance metrics. We have a tendency to aim to handle these concerns by applying real traffic patterns during a cycle-accurate simulation and by mensuration performance through established metrics for 3D NOC structures.

A. Flowchart for Proposed Routing Algorithm

In our work we are supposing to considering the source address is Sxyz – S000 and our destination address is Dxyz-D333. Now, from the flowchart (see fig 1) we are going to decode the packet (48 bit packet including source address, destination address Data bit and the processing bit is always set be binary 1). After decoding the packet the next is to find

![Flowchart](image)

Figure 1: Flowchart

![Proposed 4x4x4 mesh 3D NoC.](image)

Figure 2: Proposed 4x4x4 mesh 3D NoC.
the difference between source address with respect to the destination address. In this case, the routing algorithm finds the difference individually that means the Sx-Dx, Sy-Dy and Sz-Dz. In this, considering x-direction, they will find the difference first if the difference is less than x then it will proceed to next x-direction but if difference is greater than x then it will find the y-direction to flow the packet, similarly the process will go on and if difference is greater than y then it finds the z-direction and packet will reach the destination D333.

III. PERFORMANCE OF 3D MESH NOC

In this section, we analyse the performance of the 3D Mesh-based NoC architectures in terms of the parameters. Throughput is given in the number of accepted flits per IP per cycle. This metric, therefore, is closely related to the maximum amount of sustainable traffic in a certain network type. Any improvements in throughput in 3D networks are principally related to two factors: the number of physical links and the average number of hops. In general, for a Mesh-based NoC, the number of links is given as follows:

\[ \text{links} = N_1 N_2 (N_3 - 1) + N_1 N_3 (N_2 - 1) + N_2 N_3 (N_1 - 1) \]

(1)

Where Ni represents the number of switches in the ith dimension. For instance, in an 8 x 8 2D Mesh-based NoC, this yields 112 links. In a 4 x 4 x 4 3D Mesh-based NoC, the number of links turns out to be 144. With a greater number of links, a 3D Mesh network, for example, is able to contain a greater number of flits and therefore transmit a greater number of messages. However, only considering the number of links will not characterize the overall throughput of a network. The average hop count also has a definitive effect on throughput. Following, the average number of hops in a mesh-based NoC is given by

\[ \text{Hops} = \frac{n_1 n_2 n_3 (n_1 + n_2 + n_3) - n_3 (n_1 + n_2) - n_1 n_2}{3(n_1 n_2 n_3 - 1)} \]

(2)

Where ni is the number of nodes in the ith dimension. This equation applies both to the 4 x 4 x 4 3D Mesh. For our 4 x 4 x 4 3D Mesh and 8 x 8 2D Mesh, average hop counts are 3.81 and 5.33, respectively. There are 40 percent more hops in the 2D Mesh compared to that in the 3D Mesh. Consequently, flits in 3D Mesh need to traverse less number of stages between a pair of source and destination than the 2D counterpart. As a result of this, we expect a corresponding increase in throughput. A lower average hop count will also allow more flits to be transmitted through the network. With a lower hop count, a wormhole routed packet will utilize fewer links, thus leaving more room to increase the maximum sustainable traffic. Transport latency, like throughput, is also affected by average hop count. It is also affected heavily by the number of links and the injection load. In 3D architectures, a decrease in latency is expected due to a lower hop count and an increased number of links.

IV. IMPLEMENTATION

The investigation in routing algorithm for 3D network on chip architecture needs the simulation result to increase the performance of the system. Since ModelSim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language design. The conceptual overview of the ModelSim simulation environment. In this work, we demonstrated 3D mesh NoC in 4 x 4 x 4 configuration using our method 3D integration technology. The 3D NoC is 2 mm x 2 mm per tier. The MIT Lincoln Lab has 4 metal layers for each tier, with a metal layer between two top tiers and a metal layer on top of the entire stack. Its TSV architecture has 2.5 um x 2.5 um with 3.9 um pitch. The two bottom tiers are bonded face to face and the third tier is connected using face to back. The NoC used XYZ routing algorithm. Each router port has unidirectional links. There is a functional unit connected to each router designed using linear feedback shift register (LFSR). The design was routed with 145 MHz with the power consumption of 113.5 mW. The goal of the test chip is to validate the high level system simulator for 3D NoC they are working on. The router used XYZ routing algorithm. The node is designed as simple as possible so that mesh network can be implemented. The router has memory buffer and therefore each flit takes one cycle to travel across each router. The Figure 3 shows the simulation result.

![Simulation result](image)

Figure 3: Simulation result.

V. EXPERIMENTAL RESULT

In this work, we are going to examine with respect to the following parameter that are latency (time required to reach the packet from source to destination address), power consumption (static as well as dynamic) and number of hope (distance between node is hope) and obviously the with our proposed XYZ routing algorithm removes the congestion as well as this algorithm is fault tolerant. The comparison result of 3D Noc Architecture of routing scheme as shown in following table.
TABLE 1: EXPERIMENTAL RESULT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>latency (ns)</th>
<th>No. of Hope</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed algorithm</td>
<td>4.493</td>
<td>9</td>
<td>0.52</td>
</tr>
<tr>
<td>Existing algorithm</td>
<td>7.621</td>
<td>11</td>
<td>1.63</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

This project has investigated the routing algorithm. The intention of the current study was to determine the minimization of latency, power and number of hope. Moreover, several related topics have been covered in the beginning of this dissertation. The first step to decide the network topology that is from above thesis we choosing the mesh topology because of its simple implementation as well as node to node connection. In order to order to route the packet from source to destination, the most important we are proposed the XYZ routing algorithm which find the nearest path with respect to X, Y, Z direction towards the destination. However, most of the algorithms in the literature review have been implanted. The proposed algorithm overcomes the disadvantages. Hence, most of the works tend to reach the packet to the destination by using proposed routing algorithm. In future work we plan to inherit the algorithm considering multilevel congestion and perform their power analysis.

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VIII. REFERENCES


