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Performance Analysis of Interline Power Flow Controller for Practical Power System

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Abstract: In the fast development of the power system, the cost of the transmission lines plays a vital role in the network company. Because of the various practical constraints, the transmission lines are often only utilized for a fraction of it individual limits. To improve the economical aspects one possibility would be to add to the value of transmission lines by transport large amount of energy through those lines. One of the solutions to this problem will be a FACTS technology. An Interline Power Flow Controller (IPFC) is a converter based FACTS controller for series compensation with capability of controlling power flow among multi-lines within the same corridor of the transmission line. In this paper, it is proposed to develop the Interline power flow controller using Switching level simulation modelling. The basic characteristics of IPFC are to be analyses on two similarly dimensioned parallel transmission lines. The model has to be simulated with Matlab/Simulink program to demonstrate system behaviour of interline power flow controller. Numerical results are to be demonstrated on the practical Bus system with the Interline power flow controller model. It has to be validating that there is a possibility of regulating active power flow, reactive power flow and minimizing the power losses simultaneously with proposed IPFC parameter.

Keywords: Flexible AC Transmission System (FACTS), Voltage Source Converter (VSC), Static Synchronous Compensator (SSSC), Interline Power Flow Controller (IPFC).

I. INTRODUCTION

In general the FACTS controller can be divided in to two group converter based FACTS controller and Non converter based FACTS controller. Non-Converter based FACTS controller include Static Var compensator (SVC) and Thyristor-controlled series capacitor (TCSC) have the advantage of generating or absorbing reactive power without the use of ac capacitors and reactors. Converter based FACTS controller include STATCOM, SSSC, UPFC and IPFC which has the capable of individually control the active and reactive power flow on the transmission line. The basic concepts of FACTS controller are clearly explained in the book, 'understanding FACTS concepts and Technology of Flexible The detailed explanation about series connected. FACTS controller such as Static Synchronous Series compensator (SSSC) and Interline power flow controller given in [2, 3]. Both SSSC and IPFC have the capable of operating in capacitive/ inductive mode. The Unified Power Flow Controller (UPFC) is an combination of two FACTS device such as STATCOM and SSSC linked together with the common DC link, were as the IPFC consist of two are more than two SSSC linked together with the common DC link. Each SSSC provide the reactive power compensation to the individual line were it connected and also it has the capable of transmitting the real power from underutilized line to the overloaded line these concepts was explained in [4]. The paper [5] a simple mathematical model of IPFC was proposed for the optimal control of power flow on the transmission lines.

Mathematical models of generalized unified power flow controller (GUPFC) and IPFC and their implementation in Newton power flow are demonstrate in [6]. In the year 2002 a basic characteristic of Voltage Source Converter based Interline Power Flow Controller was discussed in paper [7] by the author Jianhong chen etal. Along with two basic control scheme, namely (i) Special Control Scheme and (ii) General control Scheme. The Special control scheme is designed for the power flow control of a transmission system with two identical parallel lines while the general control scheme can be used to solve the power flow control problem in a multi-line transmission system. Both special and general control schemes are based on the decoupled PI controller. A current source converter topology based inter line power flow controller was proposed in paper [8], along with decoupled stat-feedback control for the injected voltage with a separated dc current controller. Here the dynamic model of the system is derived and divided into a liner part and a nonlinear part. The linear part is controlled in an inner loop by a decoupled state-feedback controller. The nonlinear part is controlled in an outer loop by a PI controller which regulates the dc side current. In paper [9] the regulation model of an Interline Power Flow Controller and its control strategies at rated capacity was discussed. Rated capacity operation is important in determining the maximum power transfer capability under voltage stability conditions.

A model decomposition approach is proposed to select the best damping control input signals. The proposed technology was demonstrated on a 20-bus test system. The dispatch result shows that the IPFC improve the power transfer in the system. The author Sasan Salem proposed a two 3-level neutral point clamped voltage source converter for interline power flow controller in paper [10]. In this proposal interline power flow controller was designed to compensate the impedances of two similarly dimensioned parallel transmission lines. The behaviour of the system under various transient and load changes at the receiving-end of the transmission system was presented. The interline power flow controller has the capability in compensating both resistance and reactance of the transmission line, and maintaining the dc link voltage constant. The dc link voltage is balanced by using a balancing circuit based on zero sequence current. In this paper a detailed switching level simulation model of IPFC was developed on the Matlab Simulink environment. Here the IPFC was developed to compensate the impedance of the transmission line. An in-direct controller Strategy was developed to controller the power flow on the transmission line i.e. the power flows on the transmission line was controlled by varying the active impedance of the transmission line. The controller is also otherwise called as reactance controller as in [10]. The performance on the IPFC on the parallel transmission line was demonstrated. IEEE 30 Bus system was modelled in the Simulink and it performance was investigated with and without the IPFC. Three different case studies were carry out on the practical 30 Bus system to study the dynamic behaviour of the IPFC. Power flow analysis at base load, 10% increasing in load condition and under fault condition were carryout with and without IPFC.

II. PROBLEM FORMULATION

The demand on the power system increased gradually. The increasing in demand is fulfilled either by increasing the generation or by improving the existing system. FACTS technology is essential to alleviate some of the problem but not all of these difficulties. Converter based FACTS controller have the capability to control both active and reactive power flow on the transmission line. The objective of the FACTS controller is to maximize the power transfer capability of the transmission line. Active and Reactive power flow on a transmission line is given by

$$P = (E_1 E_2 \sin(\delta))/X \quad (1)$$

$$Q = (E1 - E2 \cos(\delta)) / X \quad (2)$$

Where E1, E2 -Magnitude of voltage at the ends of the lines X -Transmission line reactance δ - Phase angle between bus voltage and current From the above equation, it is cleared that the power transfer capability of the transmission line can be increased or decreased by adjusting the any one of the following parameter E1, E2, X and δ. SSSC and IPFC can provide the series compensation by injecting the voltage in series with the transmission line. Based on the phasor relationship between line current and injected voltage the effective reactance of the transmission line is varied. SSSC is used to control the power flow in single transmission line whereas the IPFC is used to control the power flow on a multi transmission line.

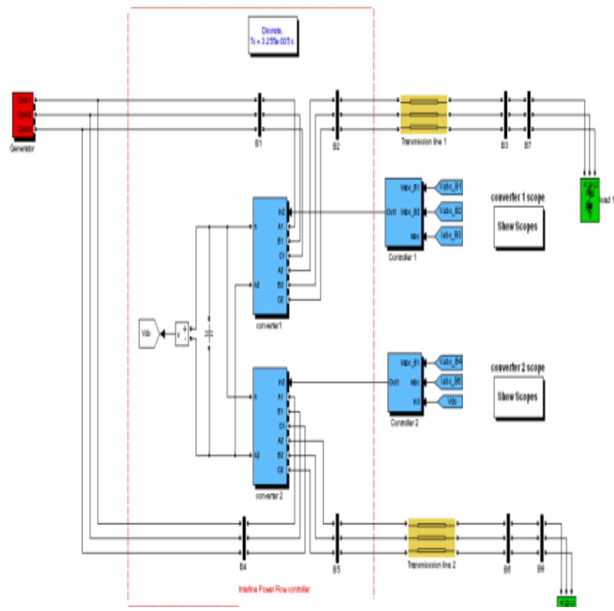

Fig.1. Detailed Simulink model of IPFC.

III. INTERLINE POWER FLOW CONTROLLER

IPFC consist of a number of DC to AC inverters, each inverter providing reactive power compensation to the different line. IPFC can also view as a combination of number of SSSC linked together at their DC terminals. A detailed Simulink model of IPFC is shown in the Fig. 1. With this configuration any of the inverter can be controlled to supply the real power to the common DC link from its own transmission line. Thus the overall surplus power can be made to utilize from the lightly loaded line to overloaded line. For analysis purpose let as consider the IPFC consist of two Voltage source converters among which converter 1 will act as the master which control the power flow on the line one independent of the line 2. Converter 2 on the line 2 is meant for maintaining the DC link voltage irrespective of variation in supply. The Simulink model consists of Generator, IPFC, Parallel transmission lines and two loads. The generator is modelled using three phase voltage source followed by impedance. The values of generator parameters are given in the Appendix I. Voltage source converters are connected in series with the transmission line through the series transformer which is shown in Fig. 2 and Fig. 3. The rating of the series transformer and the value of the DC link capacitance are given in the Appendix II. The transmission lines are constructed using the distributed parameter block available in the Simulink environment. The value of the transmission line parameter and loads on the line 1 and line 2 are given in Appendix III. IPFC's equivalent circuit and the corresponding vector diagram are shown in Fig. 4 and Fig. 5. DC link is represented by bidirectional link for active power exchange. It control characteristic is same as UPFC.

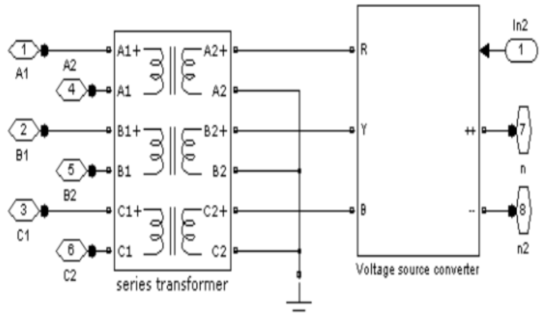

Fig. 2. Series Transformer along with VSC.

In case of UPFC the active power demand of the series converter was supplied by the shunt device. However in IPFC the active power demand of one series inverter is compensated by another series inverter. The power exchange between two inverters depending on the current flows through the transmission lines. As we know, the active power exchange between two lines can be written as

$$P_{ex} = \frac{VV_{1pq}}{X}[\sin(\delta+\rho) - \sin\rho]$$

$$P_{ex} = \frac{2V\sin(\frac{\delta}{2})}{x}\cos(\frac{\delta}{2}+\rho) \quad (3)$$

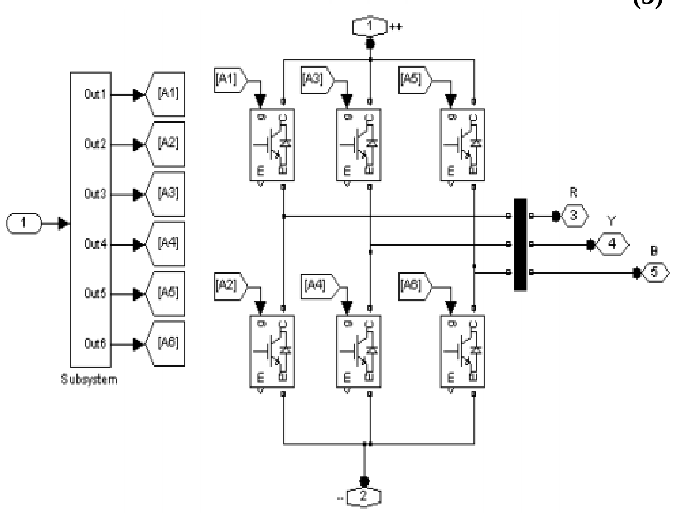

Fig. 3. Simulink model of VSC using IGBT.

IV. CONTROL STRATEGY

In this paper, the IPFC is designed to regulating the impedance of the transmission line. The primary IPFC consist of two converter system. A master converter system, that is capable of regulating impedances of Line 1. A slave converter system regulates dc-link voltage of the VSC at a desired level.

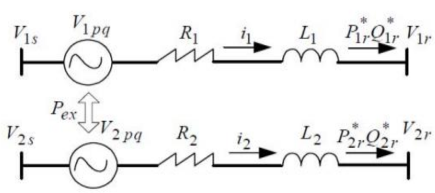

Fig. 4. Equivalent circuit of IPFC.

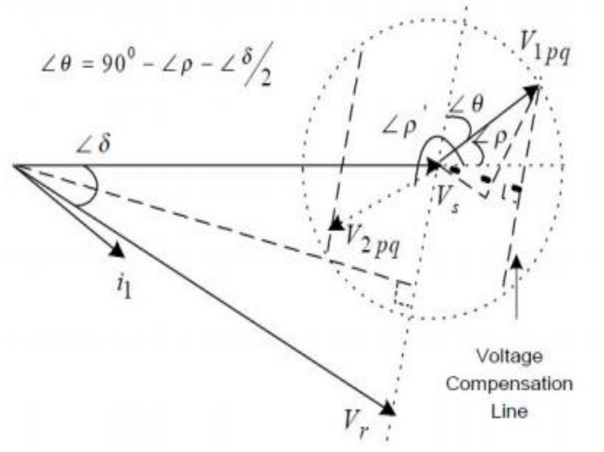

Fig. 5. Vector Diagram.

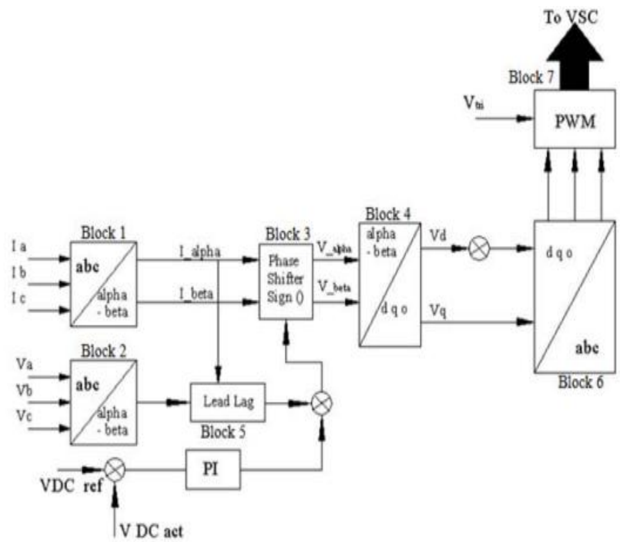

Fig. 6. IPFC slave converter system controller.

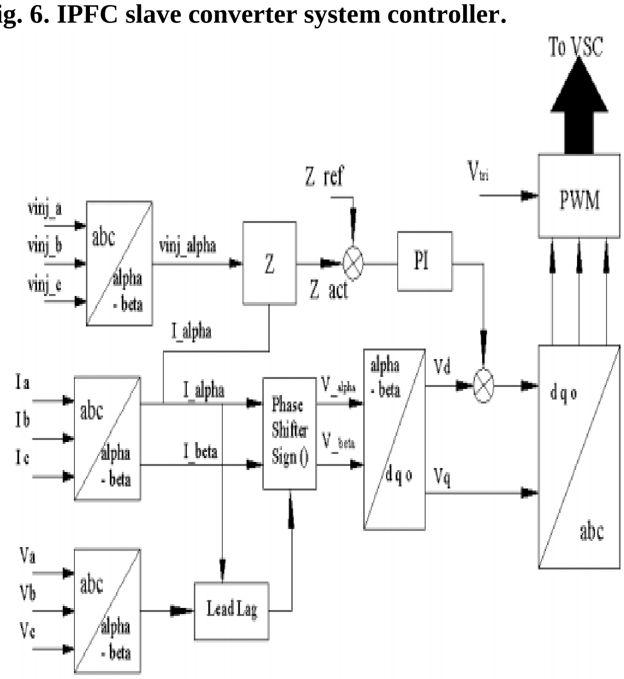

Fig.7. IPFC master converter system controller.

Fig. 6 shows the block diagram for the slave system. Block 1 is used to transform the three phase voltage injected by the VSC (V_{inj_a}, V_{inj_b}, and V_{inj_a}) in to the two phases as the equation (4). Block 2 is used to transform the three phase line currents (I_a, I_b and I_c) in to two phase I_α & I_β similar to equation (4).

$$\begin{bmatrix} V_{inj-\alpha} \\ V_{inj-\beta} \\ V_{inj-o} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{inj-a} \\ V_{inj-b} \\ V_{inj-c} \end{bmatrix} \tag{4}$$

Block 5 (Lead/ Lag Block) receives the reference signal of the line voltage V_α and from block 3 and the reference signal of the line current I_α from block 2 and computes the 90° phase shift and its sign. This information is summed with the output angle from the DC voltage controller. Block 3 receives the I_α and I_β reference signals from block 2. These signals are modulated by the sum of the signals from the DC voltage controller and Lead/ Lag blocks to generate the modified reference signals $V_{\alpha'}$ and V_β'. Block 4 is the α – β – 0 to d – q- 0 transformation block used to convert the two phase reference components in stationary frame V_α' and V_β' to two phase reference component in synchronously rotating frame V_d' and V_q' as per the equation (5). These signals are then fed to PWM trigger unit to generate the pulse.

$$\begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} * \begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} \tag{5}$$

Fig.7 shows the overall control structure of the master IPFC system. This block diagram is similar to the block diagram of the slave IPFC system and has many of the same blocks except for two major differences: (a) the dc voltage controller and (b) Impedance controller. Since the dc link voltage is controlled by the slave system, the dc voltage controller no longer needed. In order to control the impedance of the transmission line 1 impedance controller is added in addition to the slave controller. To regulate the injected impedance, an impedance Controller is used. The injected impedance Zinj-1 is compared to a reference Z_{ref} and error is fed to a PI controller. The resultant is added to the d-component of the desired reference waveform V_d'. Block 6 receives the modified d- and q- components V_d' and V_q' and transform them to three phase coordinated as per the equation 6, these signals are used as the reference signals V_a*, V_b* and c* of PWM controller. And the PWM block provides firing pulses for the VSC switched.

$$\begin{bmatrix} S_d \\ S_q \\ S_o \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t & 0 \\ -\sin\omega t & \cos\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{6}$$

V. SYSTEM DESCRIPTION

It consists of six generating units, 41-transmission lines, two VAR injecting sources, and four tap changing transformers. The base real power demand of the system is 281.43MW and the base reactive power demand of the system is 134.3 KVAR. The single line diagram of the IEEE 30 bus system is given in Appendix IV and its simulation diagram is shown in Fig. 8. The line data and the bus data are given in reference [11]. To study the dynamic behavior of the IPFC on the IEEE 30 bus system power flow analysis were carryout. The voltage profile, real power flow and reactive power flow at various buses are measured which was discussed in simulation results.

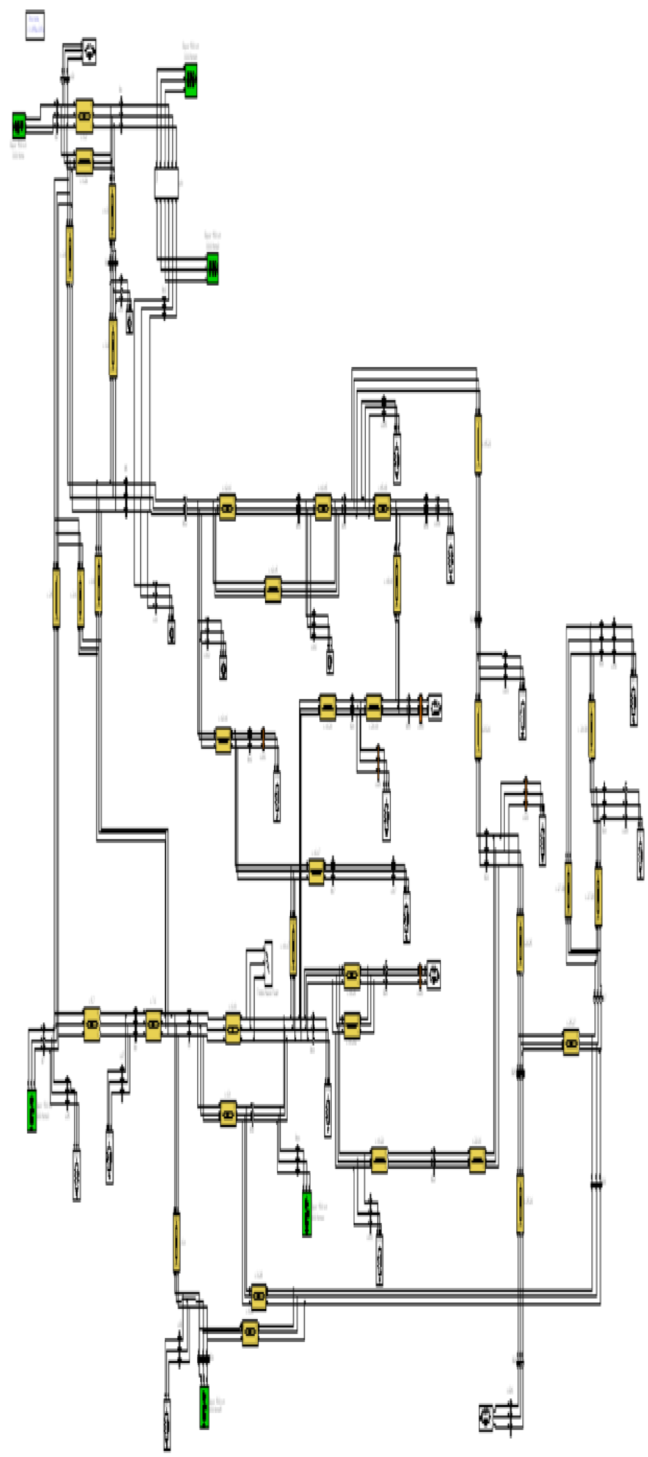

Fig. 8. Simulation diagram of IEEE 30 Bus system.

VI. SIMULATION RESULTS

Simulation results of this paper is as shown in bellow Figs.9 to 14.

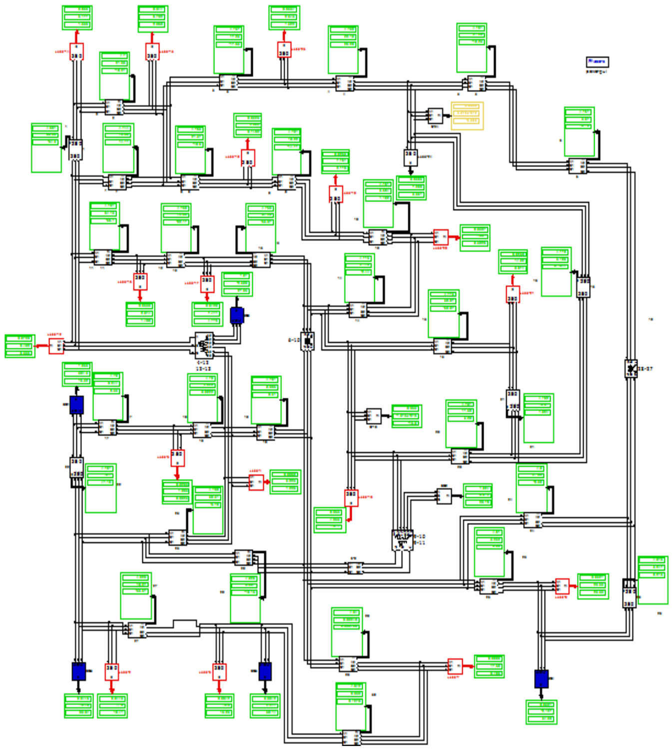

Fig.9.the Matlab/Simulink model of proposed converter.

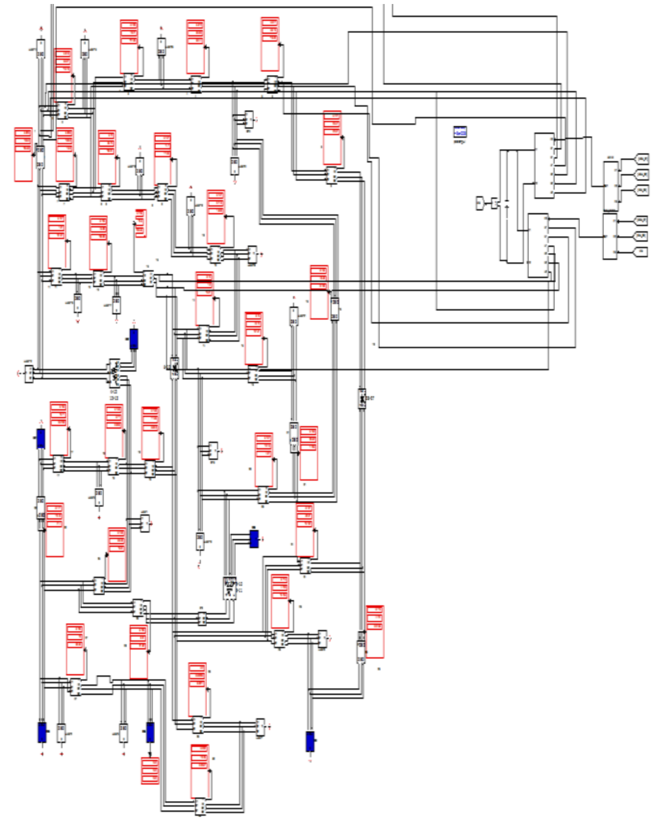

Fig.11. the Matlab/Simulink model of proposed converter under change in load condition using IPFC.

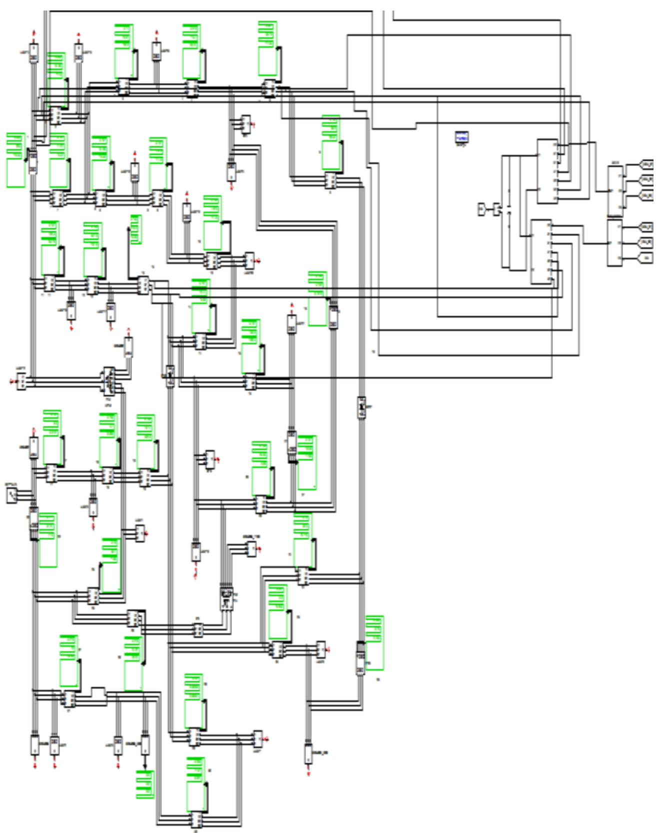

Fig.10. the Matlab/Simulink model of proposed converter under fault condition.

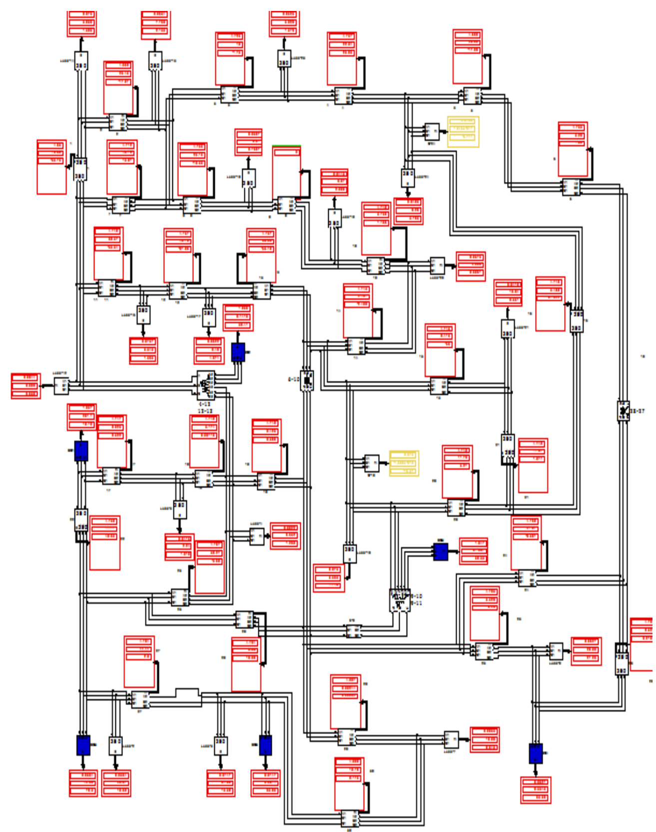

Fig.12. the Matlab/Simulink model of proposed converter under without change in load condition using IPFC.

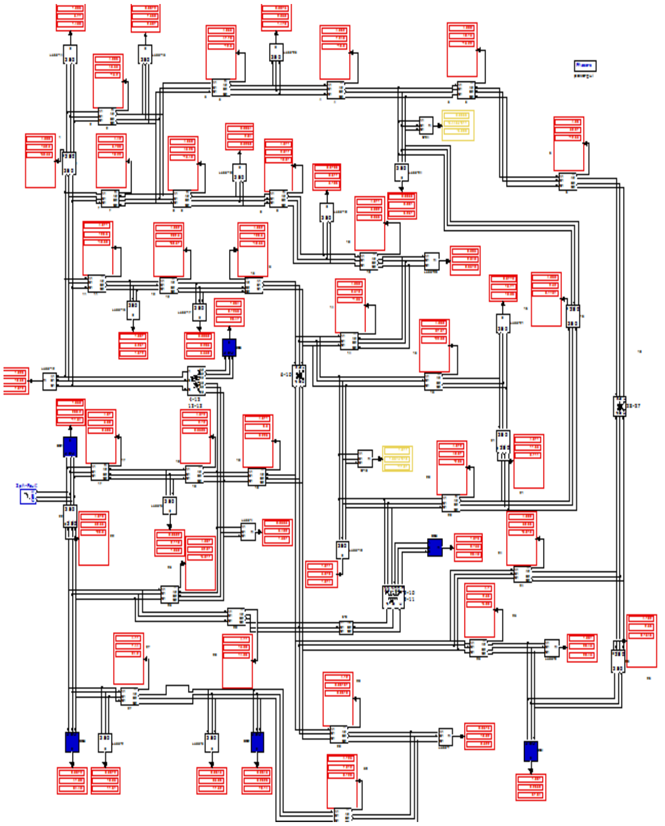

Fig.13. the Matlab/Simulink model of proposed converter under fault condition without IPFC.

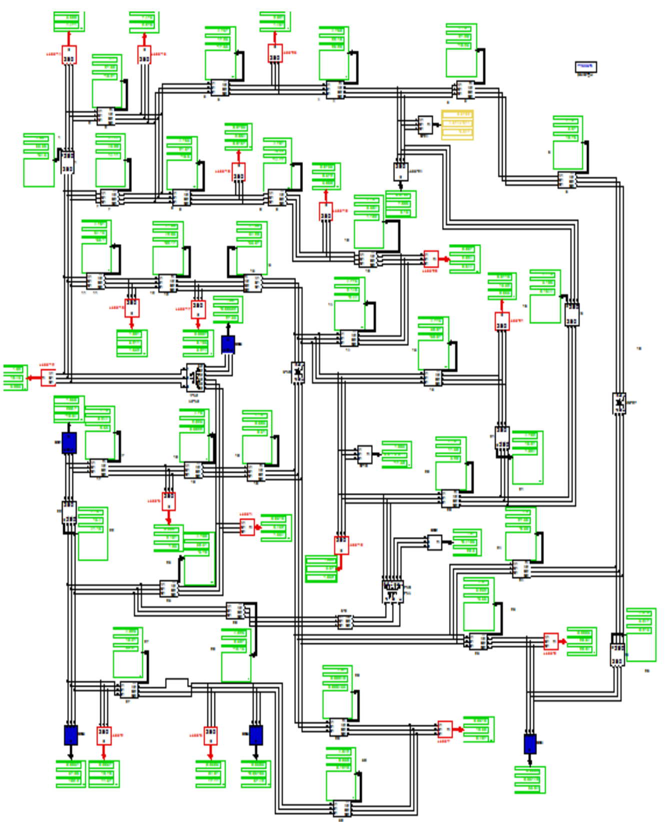

Fig.14. The Matlab/Simulink model of proposed converter under.

VII. CONCLUSION

In this paper, the detailed model of IPFC was implemented. It has the capable of exchanging the real and reactive power with the system. The performance of the IPFC on the parallel transmission lines was demonstrated. Simulation results show the effectiveness of the controller on controlling the impedance of the transmission line and hence the power flows on the chosen system. The effect of IPFC characteristic on the practical IEEE 30 bus system was demonstrated and three different case studies were carryout. From the power flow result we conclude that the Interline power flow controller increase the power transfer capability. The practical utility system with IPFC is able to maintain voltage profile within the allowable limit.

VIII. REFERENCES

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