International Journal of
Scientific Engineering and Technology Research

ISSN 2319-8885
Vol.03,Issue.02,
February-2014,
Pages:0212-0218

www.semargroup.org,
www.ijsetr.com

An On Chip Design for Prepaid Electricity Billing System

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Abstract: Electric energy meters, the direct billing interface between utilities and consumers for long, have undergone several advancements in the last decade. The conventional electromechanical meters are being replaced by new electronic meters to improve accuracy in meter reading. Still, the Indian power sector faces a serious problem of lean revenue collection for the actual electric energy supplied owing to energy thefts and network losses. One of the prime reasons is the traditional billing system which is inaccurate, slow, costly, and lack in flexibility as well as reliability. Therefore, attempts are being made to automate the billing systems. Even though more accurate and faster meter readings have seen the light of day, bill payment is still based on an old procedure. They require an individual/agent to personally come down to customer place and note the meter readings and report the amount one has to pay to the household/office. But the demand for computing power at all levels of electronic systems is driving advancements in semiconductor chip technology. So in this project we are implementing the prepaid electricity bill meter.

Keywords: Prepaid, Onchip, RTL Schematic.

I. INTRODUCTION

Electric energy meters, the direct billing interface between utilities and consumers for long, have undergone several advancements in the last decade. The conventional electromechanical meters are being replaced by new electronic meters to improve accuracy in meter reading. Still, the Indian power sector faces a serious problem of lean revenue collection for the actual electric energy supplied owing to energy thefts and network losses. One of the prime reasons is the traditional billing system which is inaccurate, slow, costly, and lack in flexibility as well as reliability. The present practice of electricity billing is manual method only. With this, the total billing is a time consuming process and it requires more manpower. The collection of billing is late procedure and so many consumers may not pay in time. Disconnecting of unpaid connections is also manual. Due to all these drawbacks we cannot have proper auditing. To overcome these drawbacks, we are implementing this project. If this system comes in our day-to-day life, it will be useful for both the Government and the public.

The objective of the project is to make the user comfortable to plan his usage of power on the beforehand as we can determine the difference between the actual power consumed and sold power easily. When system is on, it starts counting the number of units and reduces the available balance simultaneously. On completion of amount, it checks whether the backup is available or not. If it is available, it again starts counting the units. Otherwise it disconnects the line automatically with an alarm prior to that unless the system is recharged again. In this project documentation, we have initially put the definition and objective of the project as well as the analysis and design of the project which is followed by the implementation and result phases. Finally the project has been concluded successfully and also the future enhancements of the project were given in the documentation.

II. CLASSIFICATION OF IC'S

A. ASIC

An Application Specific Integrated Circuit (ASIC) is a semiconductor device designed especially for a particular customer (versus a Standard Product, which is designed for general use by any customer).

The three major categories of ASIC Technology are:

- Gate Array-Based
- Standard Cell-Based(semi custom)
- Full custom

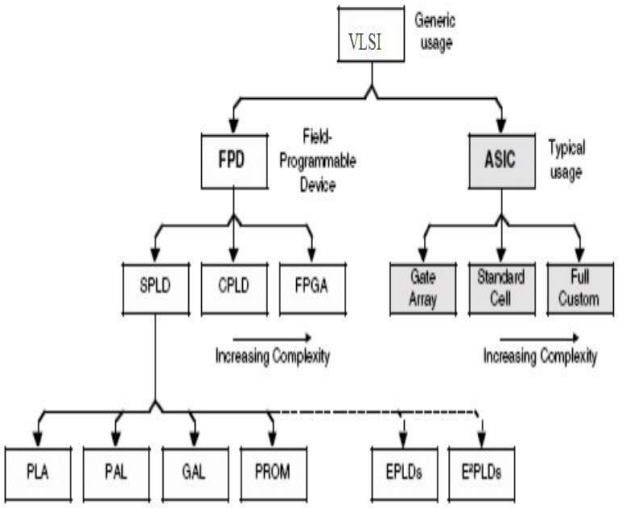


Fig1.

A. VLSI Implementation Media

- **Media requiring fabrication**

Full Custom- design and physical layout at transistor level.
Semi-Custom- design and physical layout at gate/flip-flop level.
Gate Array - design and physical layout at gate level (like standard cell but with some prefabrication of wafer) One can refer ASIC for Full Custom design and FPGA for Semi-Custom design flows. The reason being that one have the flexibility to design/modify design blocks from Vendor provided libraries in ASIC. This flexibility is missing for Semi-Custom flows like FPGA.

- **Prefabricated media**

Field Programmable Gate Arrays (FPGAs): Design at gate/flip-flop or register transfer level.
Complex Programmable Logic Devices (CPLDs): Design at gate/flip-flop or register transfer level
Programmable Logic Devices (PLDs): Design at gate/flip-flop level.

B.Comparison between FPGA, Gate array, Semi custom and full custom

	FPGA	Gate array	Standard cell	Full custom
Density	Low	Medium	Medium	High
Flexibility	Low (high)	Low	Medium	High
Analog	No	No	No	Yes
Performance	Low	Medium	High	Very high
Design time	Low	Medium	Medium	High
Design costs	Low	Medium	Medium	High
Tools	Simple	Complex	Complex	Very complex
Volume	Low	Medium	High	High

C. VLSI Design Flow

- **Top-down design** - It adds functional detail and creates lower levels of abstraction from upper levels.
- **Bottom-up design** - Creates abstractions from low-level behavior.

Good design needs both top-down and bottom-up efforts.

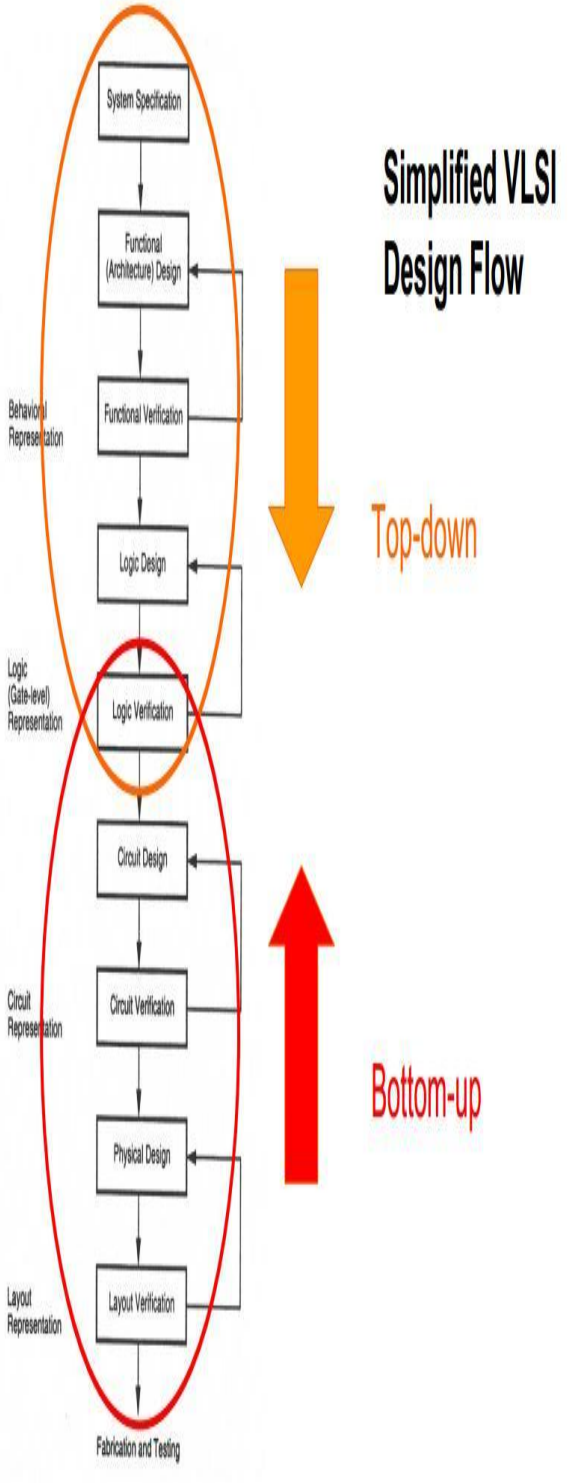


Fig2.

In this project, we are implementing top-down design flow.

III. VLSI DESIGN CYCLE

A. System Specification (Algorithmic Level)

First step of design process is to lay down the specification of the system. This is high level representation of the system.

Factors considered are:

1. Performance
2. Functionality
3. Physical dimension
4. Design technique
5. Fabrication technology

It is a compromise between market requirements, technological and economical viability.

B. Architectural Design (Register Transfer Level)

At this level the module is designed by specifying the data flow between the registers. The designer is aware of how data flows between hardware registers and how the data is processed in the design.

C. Functional Design

Main functional units of the system are identified. It also Identifies the interconnect requirements between the units. The area, power and other parameters of each unit are estimated.

The key idea is to specify behavior in terms of

1. Input
2. Output
3. Timing of each unit

Without specifying the internal structure.

The outcome of functional design is usually a timing diagram or other relationships between units. This information leads to improvement of the overall design process and reduction of complexity of the subsequent phases. Functional design provides a quick emulation of the system and allows fast debugging of the full system.

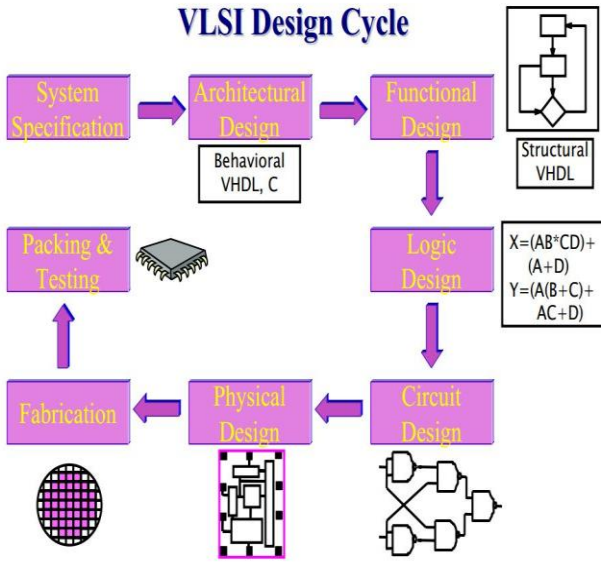


Fig3.

D. Logic Design

Design the logic, that is, Boolean expressions, control flow, word width, register allocation, etc. The outcome is called an RTL (Register Transfer Level) description. RTL is expressed in a HDL (Hardware Description Language), such as VHDL and Verilog. This description can be used in simulation and verification. As this description consists of Boolean expressions, so they can be minimized to achieve the smallest logic design.

E. Circuit Design

The purpose of the circuit design is to develop a circuit representation based on the logic design. The Boolean expression can be converted into a circuit representation by taking into consideration the speed and power requirements of the original design. After designing the circuit including gates, transistors, interconnections, etc,the outcome is called a netlist. Circuit simulation is used to verify the correctness and timing of component.

F. Physical Design

The circuit representation of each component is converted into geometric representation that is nothing but converting the netlist into a geometric representation. The outcome is called a layout.

1. Connections between different components are also expressed as a geometric pattern.
2. Exact details depends upon design rules.
3. It is a complex process and usually broken down into sub-steps.
4. Various verification and validation checks are performed on the layout during physical design.

G. Fabrication

This Process includes lithography, polishing, deposition, diffusion, etc., to produce a chip. It consists of several steps and requires various masks. Before the chip is mass produced, a prototype is made and tested.

F. Packaging, Testing

Packaging means placing together the chips on a PCB (Printed Circuit Board) or an MCM (Multi-Chip Module). Each chip is then packaged and tested to ensure that it meets all the design specifications and that it functions properly**.**

IV. OVERVIEW OF THE SYSTEM

The present system of energy billing is error prone and also time and labor consuming. Errors get introduced at every stage of energy billing like errors with electro-mechanical meters, human errors while noting down the meter reading, and errors while processing the paid bills and the due bills. There are many cases where the bill is paid and then is shown as a due amount in the next bill. There is no proper way to know the consumers maximum demand, usage details, losses in the lines, and power theft. The major drawback of a post paid system is that there is no control of usage from the

consumer's side. There is a lot of wastage of power due to the consumer's lack of planning of electrical consumption in an efficient way. Since the supply of power is limited, as a responsible citizen, there is a need to utilize electricity in a better and efficient way. The distribution company has to receive huge amounts in the form of pending bills, which results insubstantial revenue losses and also hurdles to modernization because of lack of funds. The remedy for this drawback is prepaid energy billing, which could be titled "Pay first and then use". There are clear results from many countries where a prepaid system has reduced the usage (wastage) by a large amount. Another advantage of the prepaid system is that the human errors made reading meters and processing bills can be reduced to a large extent.

The billing system is minimally able to detect power theft and even when it does it is at the end of the month. Also, the distribution company is facing many problems in terms of losses. The distribution company is unable to keep track of the changing maximum demand for domestic consumers. The consumer is facing problems like receiving due bills for bills that have already been paid as well as poor reliability of electricity supply and quality even if bills are paid regularly. The remedy for all these problems is to keep track of the consumers load on a timely basis, which will help assure accurate billing, track Maximum demand, and detect online theft. These are all the features to be taken into account for designing an efficient energy billing system. The present project Prepaid energy meter for India incorporates these features to address the problems faced by both the consumers and the distribution companies.

Thus, a Prepaid Energy Meter was introduced for embedded applications which enables power utilities to collect electricity bills from the consumers prior to its consumption came into existence in which a micro controller is interfaced with an energy metering circuit, keypad and a display to display total units and balance amount, a contactor to make or break power line, and a buzzer indicator. At the sub-station end, a PC is connected with all energy meters using any communication channel. This prepaid meter is not only limited to Automated Meter Reading [AMR] but is also attributed with prepaid recharging ability and information exchange with the utilities pertaining to customer's consumption details. Still advancements took place and efforts are being made to implement a vlsi based prepaid electricity billing system which has the following advantages.

A. Advantages of VLSI based system over embedded system:

Reliability: We have found that the reliability of an IC is a function of how many connections it has. If the function is constructed with many smaller ICs connected together, then there are many connections, and the reliability is lower. The VLSI has fewer connections, and hence higher reliability.

Speed: As all the components are placed on a single chip, the length of interconnections are smaller in VLSI and hence delay across the wires decreases which in turn increases the speed.

Power consumption: In a switching circuit most of the power is consumed switching the charge on the capacitors that connect the switches to each other. In VLSI, many small components are packed closely in a large IC such that that capacitance is much smaller among the components, and thus less power is consumed.

Less testing: If we build the same circuit out of discrete ICs and other components, each IC has to be tested (before we use it) separately as it could be used in different applications. In VLSI, the components are dedicated to a single use. Further, most are located in the middle of the VLSI and there is no access to them for testing. All you can test is the functioning of the entire circuit designed for.

Compactness: As all the components in a VLSI circuit are embedded on a single chip, the area occupied is physically less. And also the manufacturing cost is less.

V. ANALYSIS AND DESIGN

A. Energy Meter

An electric meter or energy meter is a device that measures the amount of electrical energy supplied to or produced by a residence, business or machine. The most common unit of measurement on the energy meter is the kilowatt hour, which is equal to the amount of energy used by a load of one kilowatt over a period of one hour. Electricity meters operate by continuously measuring the instantaneous voltage (volts) and current (amperes) and finding the product of these to give instantaneous electrical power (watts) which is then integrated against time to give energy used (joules, kilowatt-hours etc).

Fig.12

The most common type of electricity meter is the Thomson or electromechanical induction watt-hour meter, invented by Elihu Thomson in 1888. The electromechanical induction meter operates by counting the revolutions of an aluminum disc which is made to rotate at a speed proportional to the power. The number of revolutions is thus proportional to the energy usage. It consumes a small amount of power, typically around 2 watts. The metallic disc is acted upon by two coils. One coil is connected in such a way that it produces a magnetic flux in proportion to the voltage and the other produces a magnetic flux in proportion to the current. The field of the voltage coil is delayed by 90 degrees using a lag coil. This produces eddy currents in the disc and the effect is such that a force is exerted on the disc in proportion to the product of the instantaneous current and voltage. A permanent magnet exerts an opposing force proportional to the speed of rotation of the disc - this act as a brake which causes the disc to stop spinning when power stops being drawn rather than allowing it to spin faster and faster. This causes the disc to rotate at a speed proportional to the power being used.

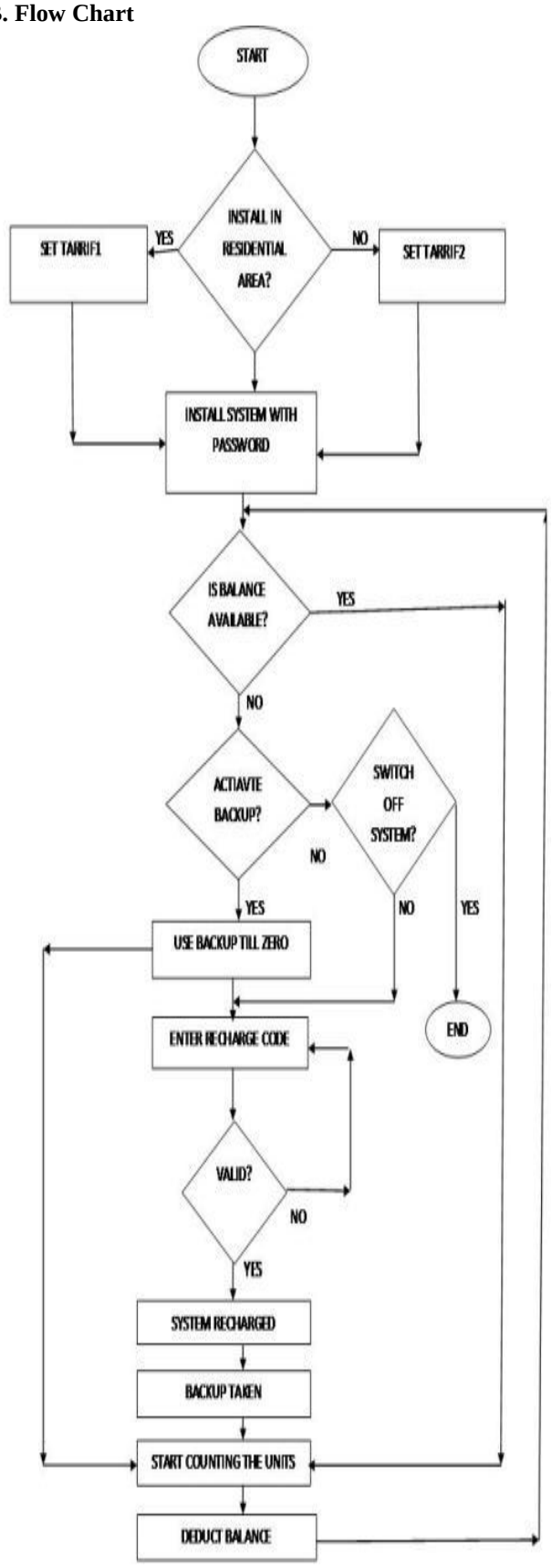
B. Reading

The aluminum disc is supported by a spindle which has a worm gear which drives the register. The register is a series of dials which record the amount of energy used. The dials may be of the cyclometer type, an odometer-like display that is easy to read where for each dial a single digit is shown through a window in the face of the meter, or of the pointer type where a pointer indicates each digit. It should be noted that with the dial pointer type, adjacent pointers generally rotate in opposite directions due to the gearing mechanism. The amount of energy represented by one revolution of the disc is denoted by the symbol *Kh* which is given in units of watt-hours per revolution. The value 7.2 is commonly seen. Using the value of *Kh*, one can determine their power consumption at any given time by timing the disc with a stopwatch.

$$P = \frac{3600 \cdot Kh}{t} \qquad (1)$$

If the time in seconds taken by the disc to complete one revolution is *t*, then the power in watts is . For example, if *Kh* = 7.2, as above, and one revolution took place in 14.4 seconds, the power is 1800 watts. This method can be used to determine the power consumption of household devices by switching them on one by one. Most domestic electricity meters must be read manually, whether by a representative of the power company or by the customer. Where the customer reads the meter, the reading may be supplied to the power company by telephone, post or over the internet. The electricity company will normally require a visit by a company representative at least annually in order to verify customer-supplied readings and to make a basic safety check of the meter.

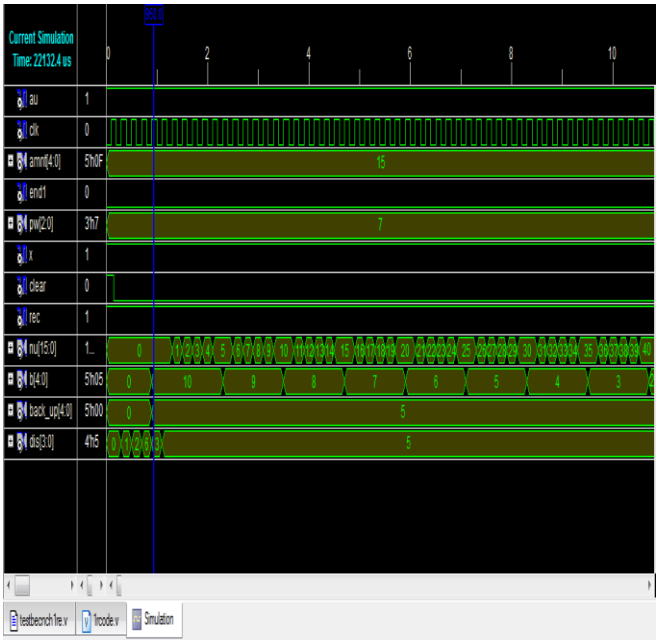
B. Flow Chart



VI. RESULTS

A. Simulated Waveform

According to the specification designed,we can see that units increment by 1 unit everytime whereas the balance deduction of 1 rupee takes place for every 5units.



B. Synthesis Report

1. Design Utilization Summary

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Total Number Slice Registers	28	9,312	1%
Number used as Flip Flops	7		
Number used as Latches	21		
Number of 4 input LUTs	7,433	9,312	79%
Logic Distribution			
Number of occupied Slices	3,876	4,656	83%
Number of Slices containing only related logic	3,876	3,876	100%
Number of Slices containing unrelated logic	0	3,876	0%
Total Number of 4 input LUTs	7,438	9,312	79%
Number used as logic	7,433		
Number used as a route-thru	5		
Number of bonded IOBs	18	232	7%
IOB Latches	2		
Number of GCLKs	2	24	8%
Total equivalent gate count for design	45,735		
Additional JTAG gate count for IOBs	864		

2. Advanced HDL Synthesis Report

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=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                    : 600
 16-bit adder                          : 200
 5-bit adder                           : 200
 5-bit subtractor                      : 200
# Registers                             : 7
 Flip-Flops                            : 7
# Latches                               : 6
 16-bit latch                          : 1
 4-bit latch                           : 1
 5-bit latch                           : 3
 7-bit latch                           : 1
# Comparators                           : 200
 5-bit comparator equal                : 200

=========================================================================
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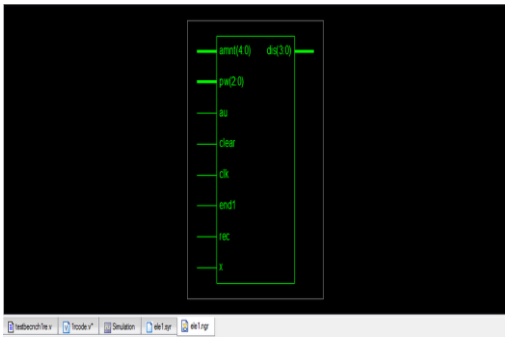
3. Timing Summary

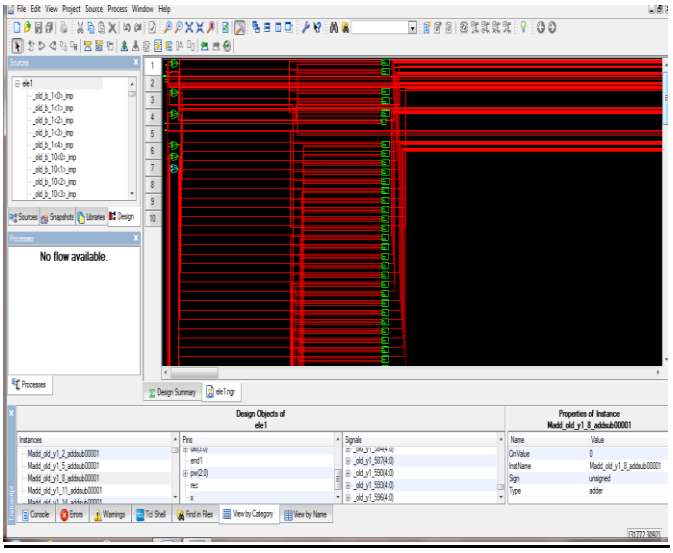
Minimum period: 775.805ns (Maximum Frequency: 1.289MHz)
Minimum input arrival time before clock: 777.129ns
Maximum output required time after clock: 5.792ns

C. RTL Schematic

1. Top module



2. Internal schematic of the top module



VII. CONCLUSION

It is estimated that approximately 9% to 18% of the power being generated in the India is stolen. Other than the loss of revenue to the distribution unit, power theft also has adverse effects on consumers and society. One effect to consumers is the increase in the fees paid by consumers who pay for power; consumer may be billed for power based upon the amount of power consumed. The other important advantage of using this system is that a tampered energy meter can be quickly detected, and power pilferage can be minimized.

The energy meter is adaptable to power tariff. Thus when there is a change in power tariff there is no need to change the meter code. The operator at the substation will calculate the number of units based on the existing tariff and recharge the meters in terms of KWh. Since the energy billing is pre-paid, the consumers will now use electricity in a better planned manner thereby reducing wastage.

VIII. REFERENCES

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