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Optimized CORDIC Design for Angle of Rotation

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Abstract: Rotation of vectors through fixed and known angles has wide applications in robotics, digital signal processing, graphics, games, and animation. But, we do not find any optimized coordinate rotation digital computer (CORDIC) design for vector-rotation through specific angles. Therefore, in this paper, we present optimization schemes and CORDIC circuits for fixed and known rotations with different levels of accuracy. For reducing the area- and time-complexities, we have proposed a hardwired pre-shifting scheme in barrel-shifters of the proposed circuits. Pipelined schemes are suggested further for cascading dedicated single-rotation units and bi-rotation CORDIC units for high-throughput and reduced latency implementations. We have obtained the optimized set of micro-rotations for fixed and known angles. The fixed-point mean-squared-error of the proposed CORDIC circuit is analyzed statistically, and strategies for reducing the error are given. We have synthesized the proposed CORDIC cells by Synopsys Design Compiler using TSMC 90-nm library, and shown that the proposed designs offer higher throughput, less latency and less area-delay product than the reference CORDIC design for fixed and known angles of rotation. We find similar results of synthesis for different Xilinx field-programmable gate-array platforms.

Keywords: VLSI, TSMC, Fixed Point, TSMC, CORDIC.

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

A Overview

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors. At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like Ultra-large-scale Integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use. Even VLSI is now somewhat quaint, given the common assumption that all microprocessors are VLSI or better. As of early 2008, billion-transistor processors are commercially available, an example of which is Intel's Montecito Itanium chip. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing new challenges such as increased variation across process corners). Another notable example is NVIDIA's 280 series GPU.

This microprocessor is unique in the fact that its 1.4 Billion transistor count, capable of a teraflop of performance, is almost entirely dedicated to logic (Itanium's transistor count is largely due to the 24MB L3 cache). Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability). Smaller physical size. Smallness is often an advantage in itself-consider portable televisions or handheld cellular telephones. Lower power consumption. Replacing a handful of standard parts with a single chip reduces total power consumption. Reducing power consumption has a ripple effect on the rest of the system: a smaller, cheaper power supply can be used; since

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less power consumption means less heat, a fan may no longer be necessary; a simpler cabinet with less shielding for electromagnetic shielding may be feasible, too. Reduced cost. Reducing the number of components, the power supply requirements, cabinet costs, and so on, will inevitably reduce system cost. The ripple effect of integration is such that the cost of a system built from custom ICs can be less, even though the individual ICs cost more than the standard parts they replace. Understanding why integrated circuit technology has such profound influence on the design of digital systems requires understanding both the technology of IC manufacturing and the economics of ICs and digital systems.

II. LITERATURE SERVAY

A. Verilog HDL

Verilog HDL is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic-level to the gate-level to the switch-level. The complexity of the digital system being modeled could vary from that of a simple gate to a complete electronic digital system, or anything in between. The digital system can be described hierarchically and timing can be explicitly modeled within the same description. The Verilog HDL language includes capabilities to describe the behavior-al nature of a design, the dataflow nature of a design, a design's structural composition, delays and a waveform generation mechanism including aspects of response monitoring and verification, all modeled using one single language. In addition, the language provides a programming language interface through which the internals of a design can be accessed during simulation including the control of a simulation run. The language not only defines the syntax but also defines very clear simulation semantics for each language construct. Therefore, models written in this language can be verified using a Verilog simulator. The language inherits many of its operator symbols and constructs from the C programming language. Verilog HDL provides an extensive range of modeling capabilities, some of which are quite difficult to comprehend initially. However, a core subset of the language is quite easy to learn and use. This is sufficient to model most applications.

B. History

The verilog HDL dialect was initially created by Gateway Design Automation in 1983 as fittings are displaying dialect for their test system item, around then ,it was a propnetary dialect. In view of the prominence of the test system item, Verilog HDL picked up acknowledgement as a usable and commonsense dialect by various creators. In a push to expand the notoriety of the dialect, the dialect was put in the general population area in 1990. Open verilog International (OVI) was structured to advance Verilog. In 1992 OVI chose to seek after institutionalization of verilog HDL as an IEEE standard. This exertion was effective and the dialect turned into an IEEE standard in 1995. The complete standard is depicted in the verilog equipment depiction dialect reference manual. The standard icalled sexually transmitted disease 1364-1995.

C. Major Capabilities

Recorded beneath are the real capacities of the verilog equipment portrayal: primitive rationale doors, for example, and, or and nand, are implicit into the dialect. flexibility of making a client characterized primitive (UDP). Such a primitive could either be a combinational rationale primitive or a successive rationale primitive. switch-level displaying primitive entryways, for example, pmos and nmos, are additionally implicit into the dialect. explicit dialect develops are accommodated pointing out pin-to-stick delays, way postpones and timing checks of a configuration. a configuration can be displayed in three separate styles or in a blended style. These styles are: behavioral style - demonstrated utilizing procedural builds; dataflow style - displayed utilizing consistent assignments, and structural style-displayed utilizing door and module instantiations. there are two information sorts in Verilog HDL: the net information sort and the register information sort. The net sort speaks to a physical association between structural components while a register sort speaks to a conceptual information stockpiling component. Fig.1 demonstrates the blended level demonstrating ability of Verilog HDL.

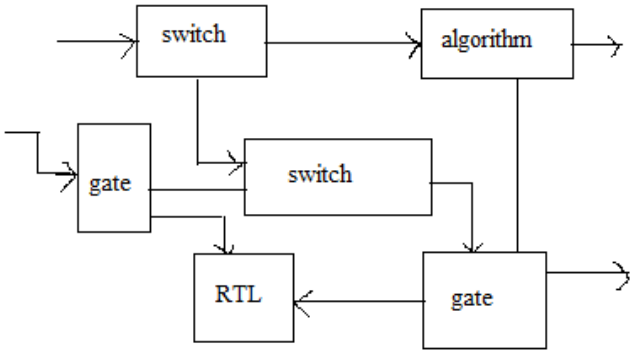


Fig.1. Mixed level of modeling.

D. Synthesis

Synthesis is the process of constructing a gate level netlist from a register-transfer level model of a circuit described in Verilog HDL. Fig.2 shows such a process. A synthesis system may as an intermediate step, generate a netlist that is comprised of register-transfer level blocks such as flip-flops, arithmetic-logic-units, and multiplexers, interconnected by wires. In such a case, a second program called the RTL module builder is necessary. The purpose of this builder is to build, or acquire from a library of predefined components, each of the required RTL blocks in the user-specified target technology. Having created a door level netlist, a rationale enhancer peruses in the netlist and streamlines the circuit for the client tagged territory and timing stipulations. These zone and timing requirements might likewise be utilized by the module developer for fitting determination or era of RTL pieces. The above figure demonstrates the essential components of Verilog HDL and the components utilized as a part of fittings. A mapping component or a development system must be given that interprets the Verilog HDL components into their relating equipment components.

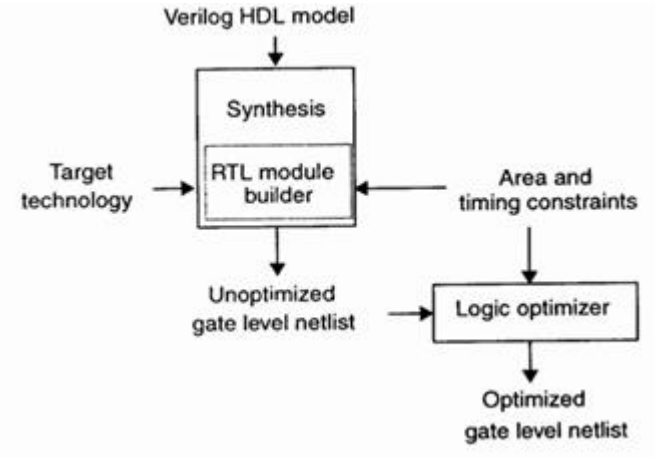


Fig.2. the synthesis process.

E. Hardware Requirements for Evaluating Elementary Functions

Universally useful micro-processors are not by any means enhanced for utilization in numerically escalated fittings applications as recorded previously. That space is adjusted by handling components which can abuse the far reaching measure of parallelism that exists in such applications, productively and at high velocity. Likewise, primary operations, for example, vector turn and trigonometric capacity assessment which happen every now and again in framework number-crunching and sign preparing when all is said in done, are exceptionally advanced in these handling components. Despite the fact that the applications of basic capacities are extremely assorted, the figuring components that perform the math controls for all of them impart some normal qualities – they must produce precise results for all points in the space, and additionally have the capacity to figure the rudimentary capacities and primary operations in an expedient way, while as of now disseminating a sensible measure of force.

The results must be gotten with high exactness for any of the plot inside the standard space of the rudimentary capacity. Procedures, for example, range decrease are useful in mapping the contention to its key area, however even so the calculation must be adaptable enough to give an exact answer any info point from inside. Power utilization has turned into an essential metric in electronic outline today, particularly as contraptions and registering gadgets contract in size. The hotness that is disseminated by the force utilization in the processing chip makes the chip hard to cool. This chip should either be run at a debased level of execution to keep it from consuming, or else extravagant and massive cooling instruments, for example, high temperature sinks or wind current must be utilized to hold the temperature down to reasonable levels. At the point when power hungry registering components are utilized as a part of customer gadgets, for example, advanced cams or Mp3 players, they empty the battery rapidly, which prompts a poor experience for the client. In any case, unnecessary force utilization restricts the execution of a number-crunching chip.

F. Rational Approximations

In the event that a polynomial Rmn(x) is continuously used to surmise a capacity over a given interim, it can be communicated as the degree of 2 different polynomials Pm(x) and Qn(x) of degree lower than R(x). On the off chance that Pm(x) and Qn(x) are polynomials of degree m and n individually, then the normal polynomial Rmn(x) made up of their proportion can generally inexact a polynomial of degree (m+n). A polynomial estimate is an exceptional instance of an objective rough guess, $Pm(x) = Rm,_0(x)$. The advantage of assessing the polynomials of lower degree will be that less expansion and increase operations are needed. What's more, objective close estimations likewise permit the numerator and denominator polynomial to be executed in parallel, consequently enhancing the execution. However this point of interest is balanced by the division operation that must be performed, and which takes quite a while to finish.

G. Mode of Operation: Origins of CORDIC

CORDIC (for Co-ordinate Rotation Digital Computer), otherwise called the digit-by-digit system and Volder's calculation, is a straightforward and effective calculation to figure hyperbolic and trigonometric capacities. It is generally utilized when no fittings multiplier is accessible (e.g., straightforward microcontrollers and Fpgas) as the main operations it requires are expansion, subtraction, bit move and table lookup. The cutting edge CORDIC calculation was initially depicted in 1959 by Jack E. Volder. It was created at the air hardware bureau of Convair to supplant the simple resolver in the B-58 assault plane's route machine. Albeit CORDIC is like numerical procedures distributed by Henry Briggs as ahead of schedule as 1624, it is streamlined for low many-sided quality limited state Cpus. John Stephen Walther at Hewlett-Packard further summed up the calculation, permitting it to compute hyperbolic and exponential capacities, logarithms, duplications, divisions, and square roots.

Initially, CORDIC was executed utilizing the parallel numeral framework. In the 1970s, decimal CORDIC got to be broadly utilized as a part of pocket adding machines, the majority of which work in parallel coded-decimal (BCD) as opposed to double. CORDIC is especially appropriate for handheld number crunchers, an application for which cost is considerably more paramount than rate (e.g., chip entryway tally must be minimized). Likewise the CORDIC subroutines for trigonometric and hyperbolic capacities can impart the vast majority of their code. The excellence of CORDIC lies in the way that by straightforward movement include operations, it can perform a few processing assignments, for example, the figuring of trigonometric, hyperbolic and logarithmic capacities, true and complex increases, division, square-root computation, arrangement of straight frameworks, Eigen esteem estimation, particular quality decay, QR factorization and numerous others. As an outcome, CORDIC has been used for applications in different regions, for example, flag and picture transforming,

correspondence frame works, apply autonomy and 3-D illustrations separated from general investigative and specialized calculation.

H. Rotation Mode

CORDIC can be utilized to compute various diverse capacities. This clarification demonstrates to utilize CORDIC as a part of revolution mode to fig.3 the sine and cosine of an edge, and expect the wanted plot is given in radians and spoke to in a settled point position. To focus the sine or cosine for an edge, the y or x direction of a point on the unit round comparing to the craved plot must be found. Utilizing CORDIC, we would begin with the vector Vo.

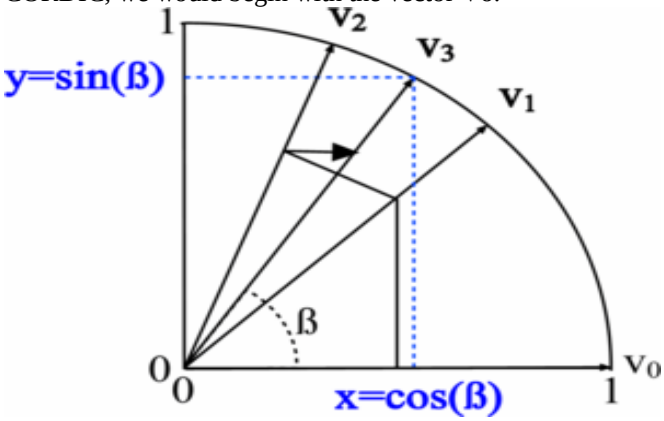


Fig.3. An illustration of the CORDIC algorithm.

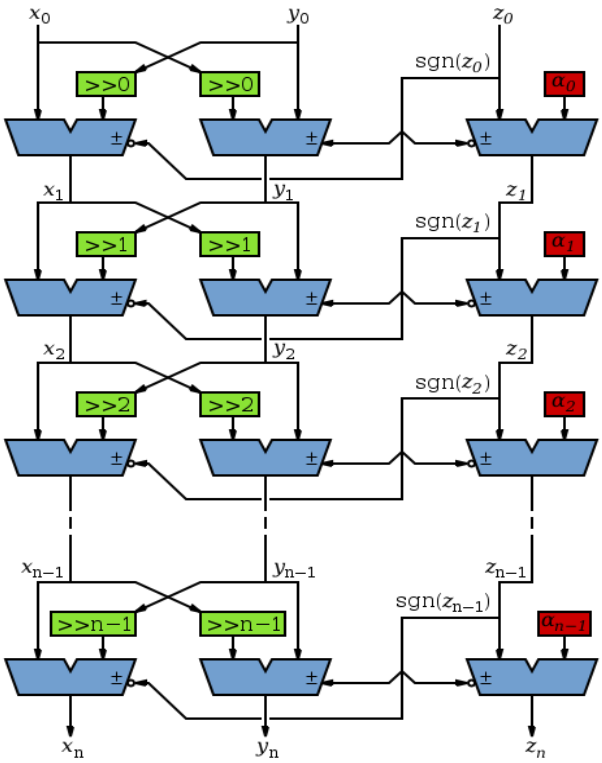


Fig.4. BIT-Parallel, Unrolled.

I. Vectoring Mode

The rotation-mode algorithm described above can rotate any vector (not only a unit vector aligned along the x axis) by an angle between –90° and +90°. Decisions on the direction of the rotation depend on β_i being positive or negative. The vectoring-mode of operation requires a slight modification of the algorithm. It starts with a vector the x coordinate of which is positive and the y coordinate is arbitrary. Successive rotations have the goal of rotating the vector to the x axis (and therefore reducing the y coordinate to zero). At each step, the value of y determines the direction of the rotation. The final value of β_i contains the total angle of rotation. The final value of x will be the magnitude of the original vector scaled by K. So, an obvious use of the vectoring mode is the transformation from rectangular to polar coordinates.

J. BIT-Parallel, Unrolled

FPGA usage is simple as registers are as of now accessible, along these lines obliging no additional fittings. Number of cycles after which the framework gives precise result can be displayed Considering clock recurrence of the framework as shown in Fig.4. when working at more prominent check period power utilization in later stages decreases because of lesser exchanging movement in each one clock period.

K. CORDIC

It is similarly the most proficient CORDIC construction modeling. In this system various emphases happen in numerous clock cycles. it is executed by embeddings enlists inside the diverse snake stages as shown in Fig.5.

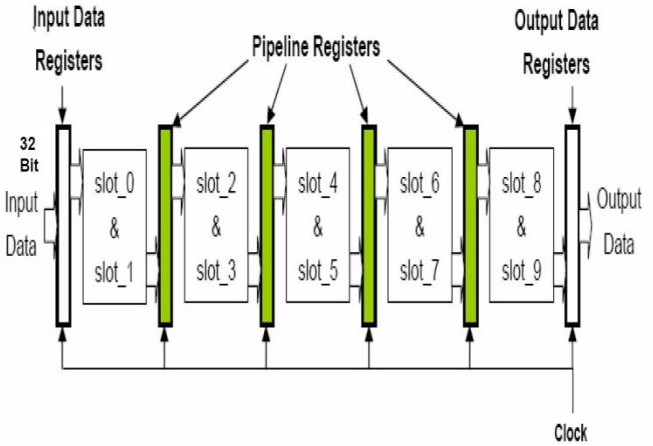


Fig.5. block graph of Pipe-lined CORDIC Architecture.

III. PROPOSED METHOD

In this paper we present the optimization schemes for reducing the number of micro-rotations and for reducing the complexity of barrel-shifters for fixed-angle vector-rotation. We also derive a cascaded pipelined circuit for this class of problem which is faster and involves less area-delay complexity than the existing approaches. The contributions of this paper are as follow. Optimized set of micro-rotations are derived for the implementation of fixed-angle vector-rotation. Shift-add operations for corresponding circuits are derived. A novel hardware pre-shifting scheme is suggested for reduction of barrel-shifter complexity. Single-rotation and bi-rotation CORDIC circuits are designed and used to derive

cascaded CORDIC for high- speed fixed-angle vector rotations. The fixed-point mean-squared-error (MSE) of the proposed CORDIC circuit is analyzed, and an efficient strategy for reducing the error is described.

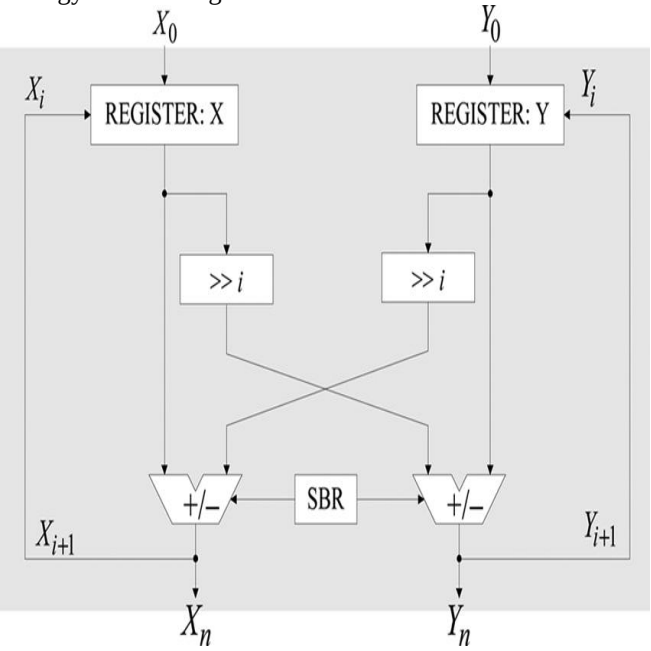


Fig.6. Reference CORDIC circuit for fixed rotations.

References CORDIC circuit for fixed rotations according to and is shown in and is fed as set/reset input to the pair of input registers and the successive feedback values a at the iteration are fed in parallel to the input registers as shown in Fig.6. Note that conventionally we feed the pair of input registers with the initial values and as well as the feedback values and through a pair of multiplexers. We show here that for rotation of a vector through a known and fixed angle of rotation using a rotation-mode CORDIC circuit, we can find a set of a small number of predetermined elementary angles for, where is the elementary angle to be used for the micro-rotation in the CORDIC algorithm, and is the minimum necessary number of micro-rotations. Meanwhile, it is well known that the rotation through any angle can be mapped into a positive rotation through without any extra arithmetic operations. Hence, as a first step of optimization, we perform the rotation mapping so that the rotation angle lies in the range.

In the next step, we minimize the number of elementary angles in the set according to the accuracy requirements. The rotation mode CORDIC algorithm of, therefore, can be modified accordingly to have the scale-factor now depends on the set The accuracy of CORDIC algorithm depends on how closely the resultant rotation due to all the micro-rotations in approximates to the desired rotation angle, which in turn determines the deviation of actual rotation vector from the estimated value. We show here that only a few elementary angles are sufficient to have a CORDIC rotation in the range, and different sets of elementary angles can be chosen according to the accuracy requirement. The simple pseudo code to optimize a set of micro-rotations is described in Algorithm 1. If the maximum accuracy which is defined as the maximum tolerable error between desired angle and approximated angle is given as an input, the optimization algorithm searches the parameters and that can minimize an objective function.

A. Bi-Rotation CORDIC Cell

We find that using only two micro-rotations, it is possible to get an accuracy up to 0.033 radian. Although the accuracy achieved by two micro-rotations is inadequate in many situations, but can be used for some applications where the outputs are quantized, e.g., in case of speech and image compression, etc., . Besides, the rotations with four and six micro-rotations can also be implemented successively by two and three pairs of micro-rotations, respectively. Therefore, we design an efficient CORDIC circuit to implement a pair of micro-rotations, and named as "bi-rotation CORDIC". The proposed circuit for bi-rotation CORDIC is shown in Fig.7. It consists of an adder-module, two 2:1 multiplexers and a sign-bit register (SBR) of two bit size. The adder-module consists of a pair of adders/sub tractors. The adders/sub tractors perform additions or subtractions according to the sign-bit available from the SBR. The components of the input vector (real and the imaginary parts of the input complex operand) are loaded to the input-registers through set/reset input.

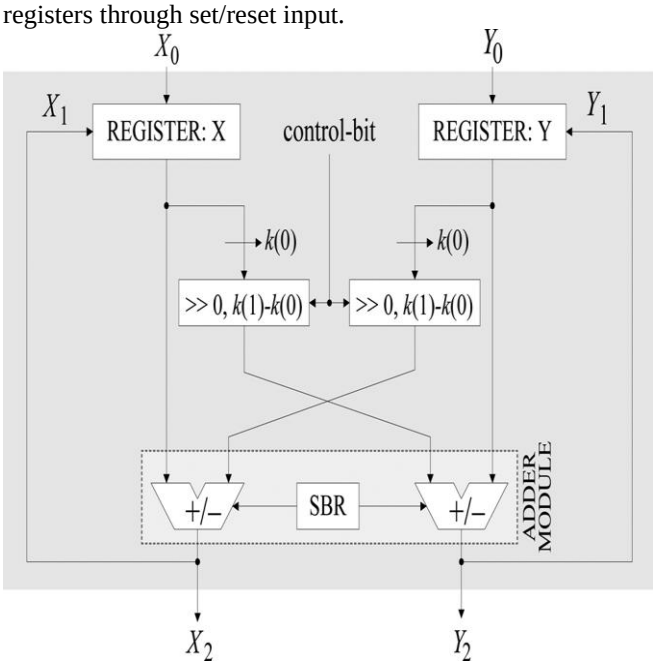


Fig.7. Hardwired pre-shifted bi-rotation CORDIC.

The output of the registers are sent in two lines where the content of the register is fed to one of the adders/sub tractors directly while that in the other line is loaded to the barrel-shifter pre-shifted by bit-locations to right by hardwired pre-shifting technique. The output of the adders is loaded back to the input registers for the second CORDIC iteration. The bi-rotation CORDIC involves only a pair of barrel-shifters consisting of only one stage of 2:1 MUXes. The

control-bit for the barrel-shifters is 0 for the first micro-rotation (no shift) and 1 for the second micro-rotation (shift through). The control bits are generated by a T flip-flop, since they are 1 and 0 in each alternate cycle.

B. Implementation of Scaling for Cascaded Single-Rotation CORDIC

The shift-add circuit for single-rotation-cascaded CORDIC is shown in . It consists of a pair of dedi- cated adders-subtractors. It does not require any multiplexer or sign-bit register. A pair of input is fed to the adder/sub- tractor from the register, where one of the inputs is obtained directly from the content of the registers, while the other input is shifted by locations to right before being fed to the adder/subtractor. The choice of adder or subtractor depends on the sign-factor in the shift-add term to be implemented by the circuit.

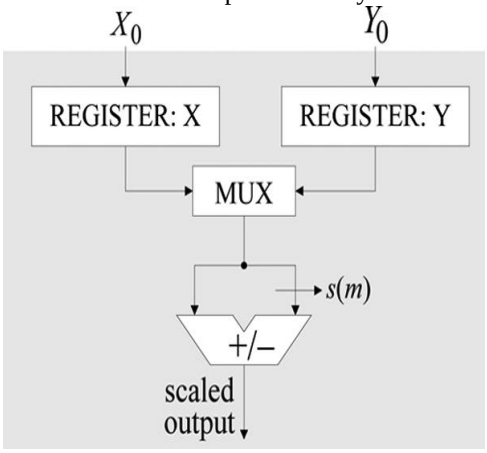


Fig.8. Time-multiplexed shift-add circuit.

C. Implementation of Scaling for Large Rotations

The scaling circuit for rotation through 43 and 45 based on is shown in Fig.8.We can implement this scaling also by simple modifications of cascaded forms of single-factor scaling circuit, two-factor scaling circuits and time-multiplexed scaling circuits of Fig.9.

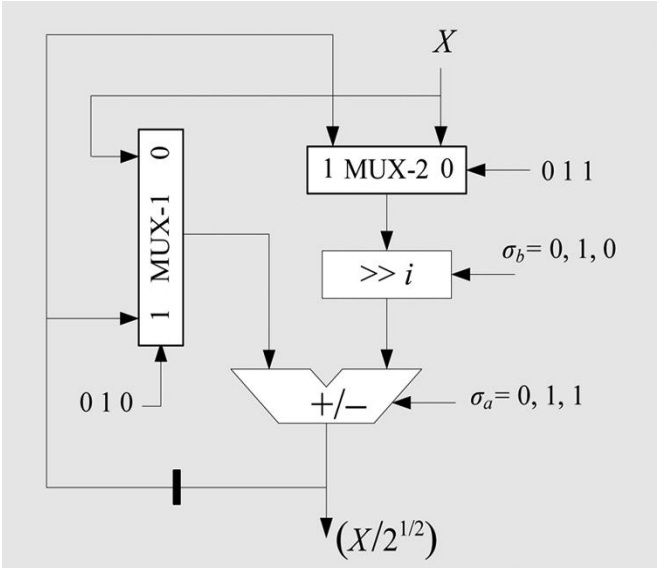


Fig9. Scaling circuit for 43 and 45 rotation.

IV. SIMULATION RESULTS

Simulation results of this paper is as shown in bellow Figs.10 and 11.

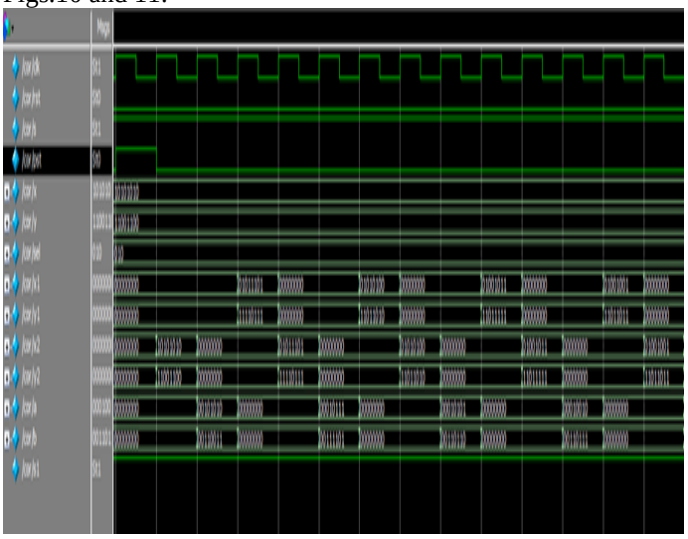


Fig.10. Simulation results of CORDIC.

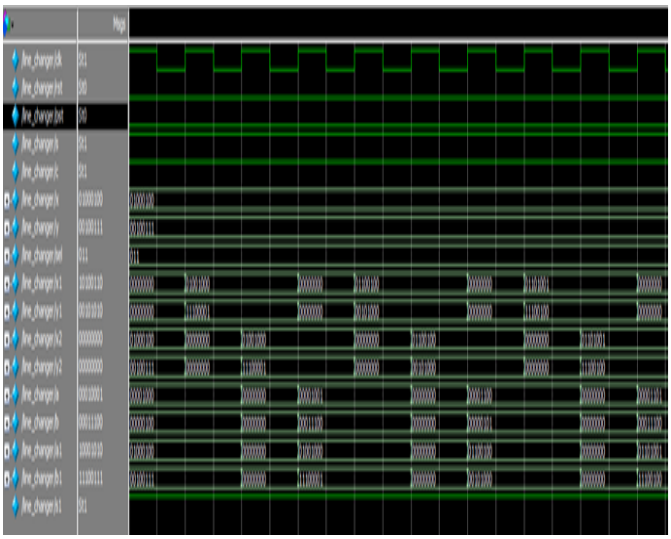


Fig.11. Simulation results of CORDIC Relations.

V. CONCLUSION

This dissertation has presented the Parallel Angle Recoding method to accelerate CORDIC rotations. The method uses range comparators to efficiently identify angle constants which can be skipped over, to reduce the number of iterations required for convergence. A unique feature of the method is that no change is required to the cycle time, so that the reduction in iteration count, translates directly to an improvement in overall latency. In order to reduce the amount of logic required, the range comparators are arranged to select the angle constants in groups known as sections. The use of sections requires evaluation cycles to be performed for each section, which adds overhead cycles to the adaptive iteration count. The number of overhead cycles can be greatly reduced by two enhancements which have been presented, which make use of functional units like a reservation station and buffers, that

are already available in the chip. In one method, the evaluation of just the first section of a rotation angle is advanced by one or more cycles. In the other method, the individual sections from two or more rotation angles are interleaved together as they pass through the CORDIC unit.

VI. EFERENCES

[1] E Costa, S Bambi, and Jose Monteiro "A New Architecture for signed Radix-2Am Pure array Multipliers" Proceedings of the2002 IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD.02)

[2] B Park, M Shin, I C Park, and C M Kyung, "Radix-4 multiplier with regular layout structure," Electronics letter, vol.34, no.15, pp.1446-7, 1998.

[3] Y K Yamanaka, T Nishidha, T Saito, M Shimohigashi, and KShimizu, A. Hitachi Ltd., Tokyo " A 3.8-ns CMOS 16x16-bmultiplier using complementary pass-transistor logic," IEEE Journal of Solid-State Circuits, vo1.25, no 2,pp.388-95, 1990.

[4] R Zimmermann and W Fichtner, Fellow, IEEE Low-Power "Logic Styles: CMOS Versus Pass-Transistor Logic," IEEE Journal Of Solid-State Circuits, vol. 32, no. 7,pp.1079-90,1997

[5] D Markovic, B Nikolic, and V G Oklobdzija, "A general method in synthesis of pass-transistor circuits," Microelectr. J,vol. 31,pp. 991-8,2000.

[6] C H Chang, J Gu, and M Zhang, "A review of O.J8-mm full adder performances for tree structured arithmetic circuits,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst. Vol. 13 pp.686-95, 2005.

[7] Massimo Alioto, Member, IEEE, and Gaetano Palumbo, Senior Member, IEEE, "Analysis and Comparision on Full Adder Block in Submicron Technology," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 10, no. 6, pp. 806-23, 2002.

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