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Low Power and Delay Error Correction Codes Based on Reed Solomon Codes

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Abstract: To avoid data corruption, error correction codes (ECCs) are widely used to protect memories. ECCs introduce a delay penalty in accessing the data as encoding or decoding has to be performed. This limits the use of ECCs in high-speed memories. This has led to the use of simple codes such as single error correction double error detection (SEC-DED) codes. However, as technology scales multiple cell upsets (MCUs) become more common and limit the use of SEC-DED codes unless they are combined with interleaving. A similar issue occurs in some types of memories like DRAM that are typically grouped in modules composed of several devices. In those modules, the protection against a device failure rather than isolated bit errors is also desirable. In those cases, one option is to use more advanced ECCs that can correct multiple bit errors. The main challenge is that those codes should minimize the delay and area penalty. Among the codes that have been considered for memory protection are Reed-Solomon (RS) codes. These codes are based on non-binary symbols and therefore can correct multiple bit errors. In this paper, single symbol error correction codes based on Reed-Solomon codes that can be implemented with low delay are proposed and evaluated. The results show that they can be implemented with a substantially lower delay than traditional single error correction RS codes.

Keywords: Reed Solomon Codes, Error Correction Codes, Single Error Correction Double Error Detection, Multiple Cell Upsets.

I. INTRODUCTION

Data corruption caused by errors is a major issue in memories. Errors can be caused for example by radiation induced soft errors that affect one or more memory cells and change their values. Other types of failures cause permanent damage such that the device no longer provides correct data. To ensure that data is not corrupted when failures occur, error correction codes (ECCs) are widely used in memories. ECCs add some additional parity check bits to each memory word such that errors can be detected and corrected. These additional bits reduce the effective capacity of the memory. Other overheads introduced by the ECC are the encoding and decoding circuitry. This circuitry has an impact also on the delay as the data has to be encoded when writing into the memory and decoded when reading from it. In most cases, the decoding is more complex than the encoding and limits the speed of the ECC. Traditionally single error correction double error detection (SEC-DED) codes are used to protect memories. These codes have a minimum Hamming distance of four such that single bit errors can be corrected while double errors are detected and not miscorrected. SEC-DED codes can be implemented with a relatively low area and delay overhead and some optimizations have been proposed. Multiple bit errors are an issue when SEC-DED codes are used. When multiple errors affect cells that are physically close, as is the case of radiation induced multiple cell upsets (MCUs) [7], SEC-DED codes can be combined with interleaving to ensure that the errors affect only 1 bit per logical word.

That is also the case when an error causes the malfunction of a device in a memory module. In that case, the word is divided in sub-blocks and an ECC is used for each of them. Then the sub-blocks are interleaved in the devices such that in a device there is only 1 bit of a given sub-block. However, the use of interleaving has an impact on the memory design and can increase area and power. For a memory module, the use of interleaving increases the number of parity check bits required, as additional bits are required per each of the sub-blocks. Finally, when multiple errors are caused by independent error events, more powerful ECCs are needed to ensure the correction of errors. A wide number of multiple bit ECCs have been proposed to protect memories. Reed Solomon (RS) codes have a distinct feature when compared with the other codes: they are not binary. They use symbols from a Galois Field such that each symbol is represented by multiple bits. Therefore a SEC RS code can correct multiple bit errors as long as they affect a single symbol. This is very attractive for memory modules as when the number of bits in the devices matches those of the symbols

in the RS code, failures in one device can be corrected. In fact, for this reason RS codes are commonly used to protect main memories in computer systems for space applications. In general, the data that forms an RS codeword are considered as polynomial coefficients with values belonging to the Galois Field. The polynomial corresponding to a codeword is a multiple of a specific polynomial, called generator polynomial g(x). Interested readers can refer to a classical textbook on error control codes.

II. EXISTING METHOD

Reed Solomon codes are a subclass of non paired BCH codes developed with images from a Galois Field GF(q) where q is regularly a force of two. For; m bit images are utilized to build the code. A RS code has the accompanying parameters: most extreme square length n = q-1, number of equality check images n-k= 2t and least separation dmin = 2t +1. Each one of those parameters are communicated as far as q-ary images. As an image has m bits, the most extreme piece length in bits is m(q-1) and the quantity of equality check bits 2mt. Whenever t=1, the base separation is three and thusly the code can adjust single image mistakes. These blunders can influence numerous bits the length of every one of them have a place with the same image. RS codes are generally communicated as RS(n, k, m). The equality check lattice for a RS code is developed as appeared in mathematical statement (1) where a will be a primitive component in GF(q):

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & \alpha & \alpha^2 & \cdots & \alpha^{n-1} \\ 1 & \alpha^2 & (\alpha^2)^2 & \cdots & (\alpha^2)^{n-1} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 1 & \alpha^{2t} & (\alpha^{2t})^2 & \cdots & (\alpha^{2t})^{n-1} \end{bmatrix} \quad \textbf{(1)}$$

For a single error correction code only two parity check symbols are needed and therefore the matrix is simply:

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & \cdots & 1 \\ 1 & \alpha & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} \end{bmatrix}. \quad \textbf{(2)}$$

The unraveling of a SEC RS code begins with the calculation of the disorder vector, which for a piece r is basically:

$$s = H.r \quad \textbf{(3)}$$

The disorder vector can be utilized to recognize blunders as takes after. When every one of the bits in the vector are zero, no blunder is recognized. At the point when no less than 1 bit is one, a blunder is recognized and hence mistake amendment must be performed. The deferral and intricacy of disorder calculation relies on upon the estimations of the equality check network. For instance, for the primary line of (1) the count is basic as all qualities are ones while for the second a few duplications are required. Accepting a solitary image blunder e in position i in the piece, the disorder would be:

$$s = \begin{bmatrix} e \\ e \cdot \alpha^i \end{bmatrix} \quad \textbf{(4)}$$

In this manner for a solitary image mistake if the second image of the disorder is partitioned by the main, the quality is acquired. The blunder is then situated by finding the example of the remainder and can be at last redressed by subtracting e from the ith image. Rectification in this way requires one division and one logarithm operation. As the images are from GF(q), all operations are done over that field. This implies the interpreting turns out to be more intricate as develops. From comparisons (2) and (4) it is straightforward which is the greatest piece length of a SEC RS code. Assume that we need to include a further section in the structure to the lattice in mathematical statement (2). Since in the Galois Field , a mistake in this section would deliver the same disorder of a blunder in the main segment of the equality check framework. This associating implies that there are uncorrectable blunders when the codeword length surpasses n. Nonetheless, there is a surely understood expansion of the SEC RS code, to permit amplifying the most extreme square length up to q þ 1 images. This should be possible including the sections and the H network, acquiring the accompanying framework:

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & \cdots & 1 & 1 & 0 \\ 1 & \alpha & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} & 0 & 1 \end{bmatrix} \quad \textbf{(5)}$$

The sections of the H network are still directly autonomous and the translating system must be changed to deal with the cases in which one of the disorders is zero, that compare to a blunder in the last two codeword images.

Disadvantages:

- The interpreting of SEC RS codes requires various complex operations over GF(q) particularly for mistake remedy where division and logarithm should be executed.
- Syndrome calculation just requires increases and augmentations and its deferral relies on upon the estimations of each of the lines in the H network.

Subsequently to decrease information access delay by performing mistake identification first and continue to redress just when there are blunders, so that the information access deferral will be constrained when expected to figure the disorder. i.e., use proposed codes.

III. PROPOSED METHOD

Two altered SEC RS codes are displayed to lessen the deferral for encoding and for blunder discovery. The primary alteration tries to enhance the equality check framework to decrease the postponement for encoding and disorder calculation. The second joins the first with an augmentation of the utilization of RS codes for a given an estimation of q to empower longer piece lengths. This decreases the encoding and unraveling postpone further as the augmentations and other number juggling operations are done over a less complex Galois Field.

A. Optimizing Parity Check Matrix

For a SEC-RS code, the calculation of the equality check grid is unequal. The augmentation of the primary line of the framework for a piece r requires no increases on the Galois Field while the second requires n-1 duplications on the Galois Field. The initially proposed alteration to RS codes tries to adjust the intricacy of both counts. This is finished by utilizing the accompanying equality check grid:

$$H = \begin{bmatrix} 1 & 1 & \alpha^{-2} & 1 & \cdots & \alpha^{-(n-1)} & 1 & 0 \\ 1 & \alpha & 1 & \alpha^{3} & \cdots & 1 & 0 & 1 \end{bmatrix} \quad \textbf{(6)}$$

and the corresponding parity generator matrix:

$$G = \begin{bmatrix} & & & I_k & & \\ 1 & 1 & \alpha^{-2} & \cdots & \alpha^{-(n-2)} & \\ 1 & \alpha & 1 & \cdots & 1 & \end{bmatrix} \quad \textbf{(7)}$$

The framework of mathematical statement (6) can be specifically acquired from comparison (5) duplicating the i-th segments, when i is even, for the quality α^(- 1). The adjusted code is still a SEC code as the segments are straightly autonomous. With this adjustments the calculation of each of the check images amid the encoding process, and of the disorder images amid the translating process, requires the same number of duplications. This diminishes the length of the basic way and along these lines brings down the postponement. The deciphering for the proposed codes is like that of SEC RS codes. Assume to have a blunder of size e in the ith image. In the event that the disorder vector , then i = n-1 and e = S0. On the off chance that , then i = n and e = S1. Something else, the disorder vector will be the point at which i is even and when i is odd. In this way, for all i < n_ 1 and we can process the mistake area. At that point we can recover eS0 for even estimations of i, and e S1 for odd estimations of i and right the mistake. This procedure requires one division and one logarithm, the same as the deciphering of conventional SEC RS codes.

B. Extension to longer block lengths

Another component that effects the postponement of RS encoders and decoders is the span of the Galois Field that is utilized to develop the code. This is because of the expansion of the many-sided quality of the number-crunching operations for bigger Galois Fields. As clarified in the past area, for a given GF(q) the greatest piece size of a customary RS code is q _ 1 images. This restriction constrains the utilization of bigger Galois Fields for vast square sizes in this way expanding the deciphering delay. This issue can be fathomed by utilizing a changed SEC RS code with the accompanying H lattice:

$$H = \begin{bmatrix} \alpha & 1 & 1 & \alpha^{2} & 1 & 1 & \cdots & 1 & 0 & 0 \\ 1 & \alpha & 1 & 1 & \alpha^{2} & 1 & \cdots & 0 & 1 & 0 \\ 1 & 1 & \alpha & 1 & 1 & \alpha^{2} & \cdots & 0 & 0 & 1 \end{bmatrix}. \quad \textbf{(8)}$$

With this change, the piece length can be up to 3(q-1) images. The extra line permits to separate between disorder vectors that generally could have the same disorder esteem.

The translating is like the past case. Assume we have a blunder of size e in the ith image. On the off chance that the disorder vector contains two zeros, the blunder is in the comparing check image. Something else, two disorder images will have the same worth, relating to the blunder greatness e. The third disorder image (the one with a worth not the same as the other two) will have an estimation of and along these lines the blunder area can be gotten. All the more definitely, on the off chance that we signify Sa (with a ¼ 0, 1 or 2) this disorder image, the area i is The disentangling takes again a few correlations, a division and a logarithm.

Advantages:

- Reduce the mistake identification delay.
- Reduce the deferral to get to the information when the plan of performing blunder recognition first and continuing to the following periods of interpreting just if there are mistakes is utilized.

Applications:

- These are utilized to secure primary recollections in PC frameworks for space applications.

IV. RESULTS

Results of this paper is as shown in bellow Figs.1 to 4.

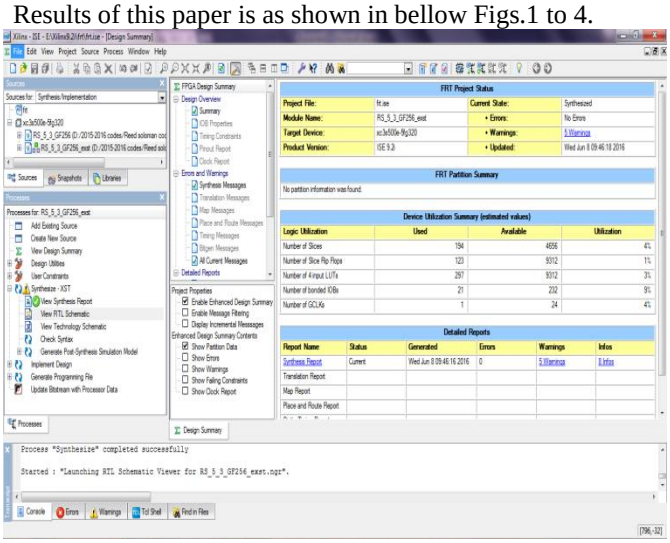

Fig. 1. Design summary of Existing method.

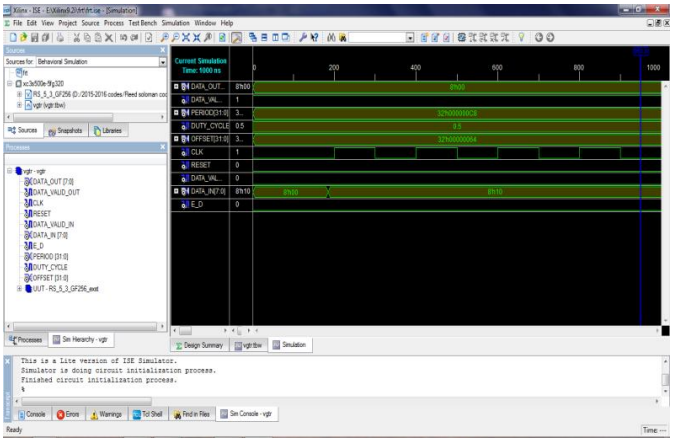

Fig. 2. Simulation of Existing method.

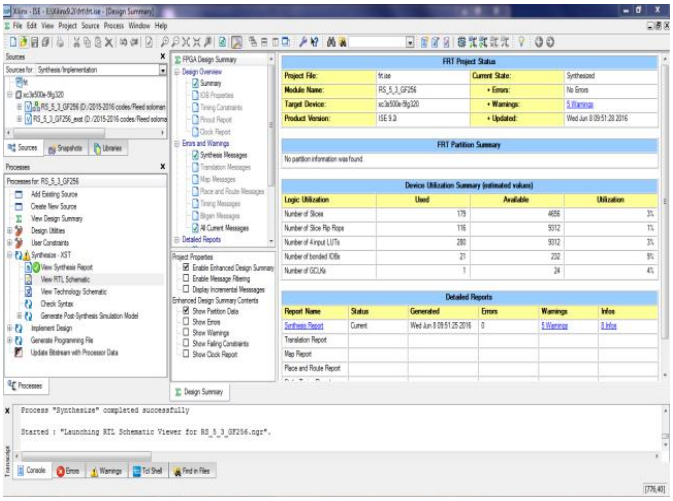

Fig.3. Design summary of Proposed method.

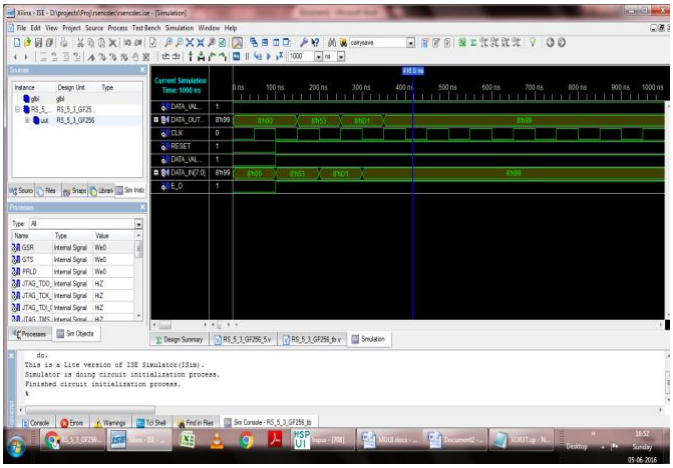

Fig.4.Simulation of Proposed method.

TABLE I: Comparison Between Existing Method And Proposed Method

Logic Utilization	Existing Method	Proposed Method
No of slices	194	179
No of slice flip flops	123	116
No of 4 input LUTs	297	280
No of Bounded IOBs	21	21
No of GCLKs	1	1
Delay (n sec)	3.40	3.30
Power (μ watts)	0.66	0.62

V. CONCLUSION

In this project, new codes in light of changes of single blunder adjustment Reed Solomon (SEC RS) codes have been proposed with the goal of lessening deferral. The codes have been executed and assessed. The illustrations utilized for assessment compare to genuine arrangements generally utilized as a part of memory modules. For those, the proposed codes empower noteworthy deferral diminishments in encoding and disentangling delay. This makes the adjusted codes appealing for rapid recollections. Future work will consider the evaluation of the proposed codes to ensure different types of memory like for examples caches.

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