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Design and Simulation of FMO/Manschester/Miller Encoder for Short Range Applications

B.VIJAYA BHARGAVI[1], G. PARAMESHWAR[2]

[1]PG Scholar, Dept of ECE(DSCE), Lords Institute of Engineering & Technology, Hyderabad, Telagana, India,
E-mail: bhargavi.vijji92@gmail.com.

[2]Associate Professor & HOD, Dept of ECE, Lords Institute of Engineering & Technology, Hyderabad, Telagana, India,
E-mail: paramesh.gujjula@gmail.com.

Abstract: The Dedicated Short-Range Communication (DSRC) is an emerging standard to push the vehicular communication into modern automotive industry. The DSRC standard generally applies FM0, Manchester, Miller encoding to reach DC-balance. In this paper we proposed a new architecture of Encoding of data by integrating all the three encoder into an one Encoder. SO, the user can encode the data by using either with the FMO, Manchester or Miller encoder depending on requirement he uses. These architecture was designed using the Verilog Coding. The simulation and synthesis reports are generated to the proposed architecture was shown.

Keywords: Dedicated Short-Range Communication (DSRC), FM0, Manchester, Milller.

I. INTRODUCTION

The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobiles for safety issues and public information announcement [2], [3]. The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the toll collecting is electrically accomplished with the Contactless IC-card platform.

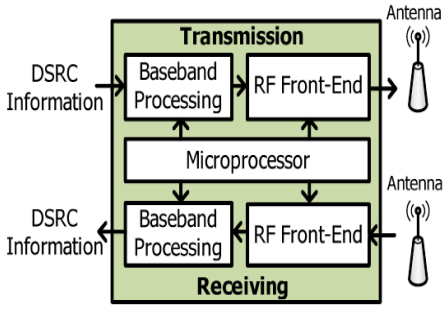

Fig1. DRSC Transceiver.

Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The system architecture of DSRC transceiver is shown in Fig1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna.

II. FMO ENCODING

FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding, the signal to be transmitted and done according (Figure 2), to the following rules,

- It inverts the phase of the base band signal at the boundary of each symbol. For representing logic '0' level, it inverts
- The signal at the mid of the symbol. For representing logic '1' level, it constant voltage occupying an entire bit window.

A FM0 coding example is shown in Fig. 3. At cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

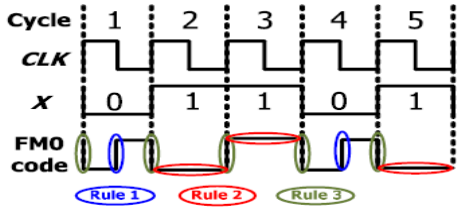

Fig2. FMO Encoding.

III. MANCHESTER ENCODING

The Manchester coding example is shown in Fig3. The Manchester code is derived from X (XOR) CLK. The Manchester encoding is realized with a XOR operation for CLK and X. The clock always has a transition within one cycle, and so does the Manchester code no matter what the X is. Manchester code ensures frequent line voltage transitions, directly proportional to the clock rate; this helps clock recovery. The DC component of the encoded signal is not dependent on the data and therefore carries no information, allowing the signal to be conveyed conveniently by media (e.g.Ethernet) which usually do not convey a DC component.

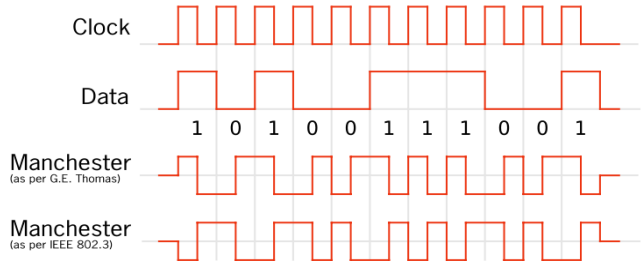

Fig3. Manchester waveform.

IV. ARCHITECTURE FOR FM0 AND MANCHESTER ENCODING TECHNIQUES

The literature proposes a VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature further replaces the architecture of switch in by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The literature proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator. Its maximum operation frequency is about 192 MHz. Furthermore, combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

V. FM0 AND MANCHESTER ENCODING

To make an analysis on hardware utilization of FM0 and Manchester encoders, the hardware architectures of both are conducted first. As mentioned earlier, the hardware architecture of Manchester encoding is as simple as a XOR operation. However, the conduction of hardware architecture for FM0 is not as simple as that of Manchester. How to construct the hardware architecture of FM0 encoding should start with the FSM of FM0 first. As shown in Fig. 5(a), the FSM of FM0 code is classified into four states. A state code is individually assigned to each state, and each state code consists of A and B, as shown in Fig. 2. According to the coding principle of FM0, the FSM of FM0 is shown in Fig. 5(b). Suppose the initial state is S1, and its state code is 11 for A and B, respectively. If the X is logic-0, the state-transition must follow both rules 1 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state, as shown in Table II. A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1) and the B(t − 1), respectively. With this transition table, the Boolean functions.

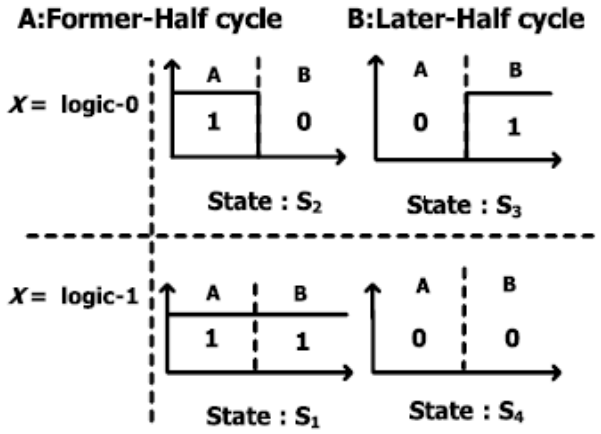

Fig4. State Diagram.

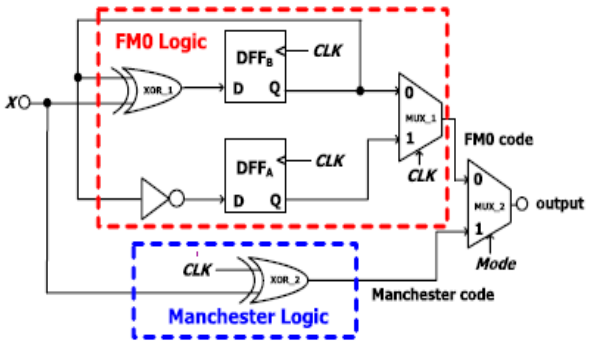

Fig5. FM0 and Manchester encoding techniques.

A. FM0 Manchester encoding techniques:

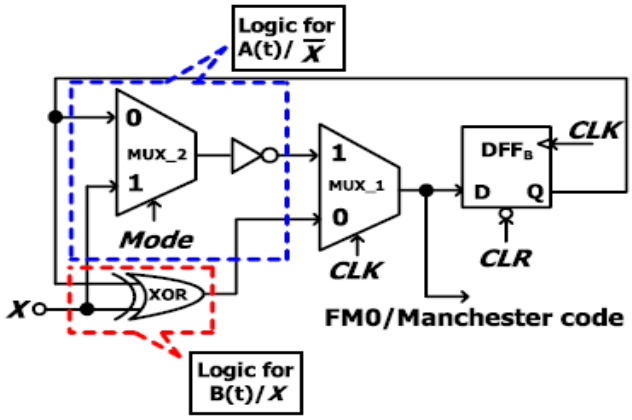

Fig6. Unbalance circuit.

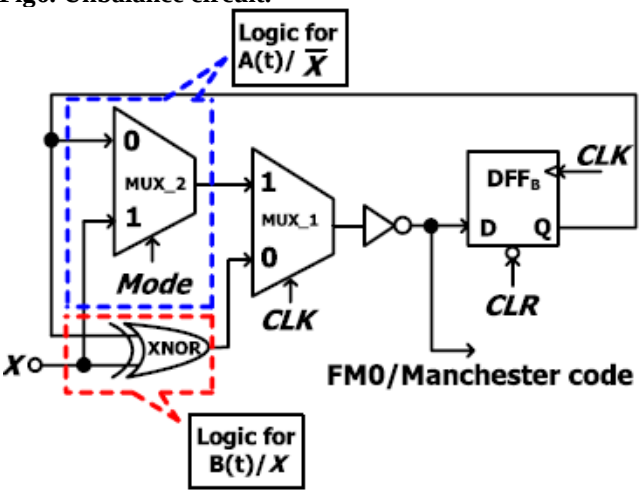

Fig7. Balance circuit.

VI. MILLER ENCODING TECHNIQUE

Miller encoding is also known as delay encoding. It can be used for higher operating frequency and it is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is 1. While using the Miller delay, noise interference can be reduced. The block diagram has a d flip flop, t flip flop, NOT gate, and XOR gate. Where the input is A_in and CLK, then the output is a Miller output. For example, if the input is 0 and the clock, given the XOR operation has done that, is A_in CLK , therefore 0 plus a positive edge clock produces the output as 0. Given to d flip flop, the clock has inverted, and after that output is given to t flip flop it inputs and flip flop output, which is 0. Then the TFF is toggle FF, which produces the Miller output as 1.

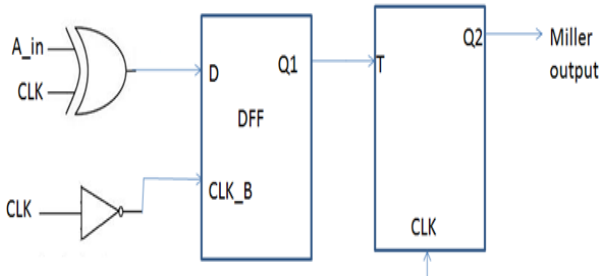

Fig8. Block Diagram of Miller Encoding.

Design of FMO Manchester and Miller in One Module:

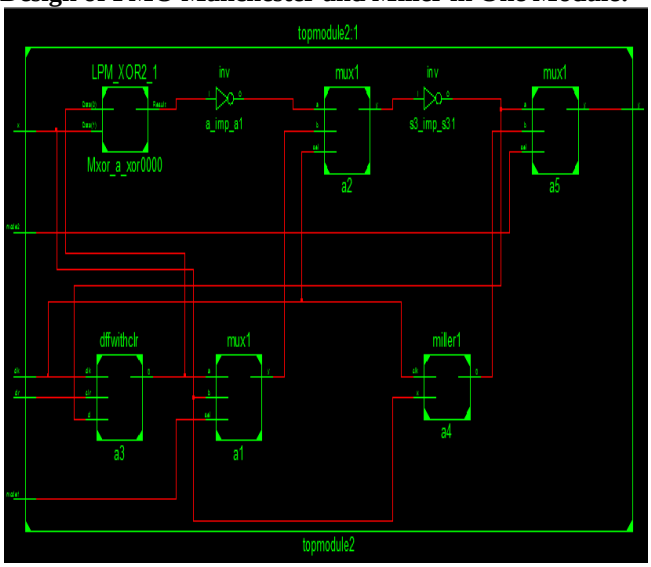

Fig9. RTL design flow of Proposed Encoder.

From the previous logics of FMO/Manchester was taken as same architecture for this we add a Miller Encoding by adding another MUX to it. SO the user can select the type of encoding he wants with the two selection lines. The selection truth table was shown below

Table1. Transition Table of proposed Encoder

Mode1	Mode2	Clear	Output
0	0	1	FMO
1	0	0	Manchester
1	X	x	Miller

VII. SIMULATION

The below waveform shows the proposed encoder by choosing the Mode1, Mode2 and Clear inputs we can change the type of Encoding in the architecture. These simulation was carried out using Modelsim6.5e Simulator

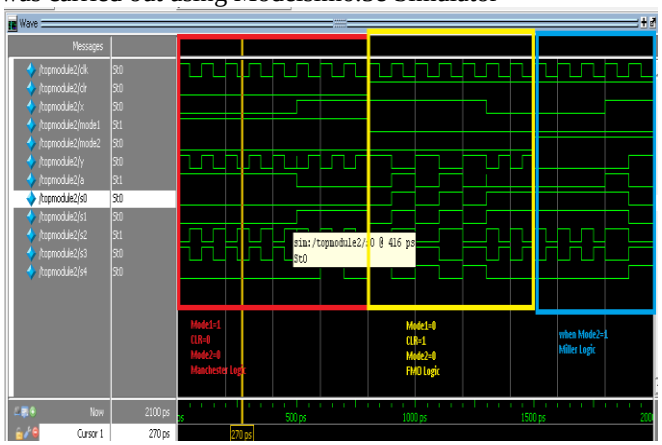

Fig10. Simulation of Proposed Encoder.

VIII. CONCLUSION

In this paper, we have designed the architecture of a New Proposed Encoder which integrates the FMO, Manchester and the Miller Encoding Techniques. In the First part we have Integrated the FMO/ManchesterTechniques and applied

the Similarity Logic Oriented Simplification technique (SLOS) technique for reduction of the Hardware. Then after we integrated the reduced FMO/Manchester technique with the Miller Encoder. Such that user can have choice of Encoding their data with any Encoder by choosing te Mode was Proposed in this paper.

IX. REFERENCES

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Author's Profile:

B.Vijaya Bhargavi Graduated as an Electronics & Communication of Engineering and technology in2014 from Vanjari Seethaiah Memorial College of Engineering, Hyderabad And pursuing M.TECH Digital systems and computer electronics from Lords institute of engineering and technology. Interest in VLSI low power.

G.Parameshwar, graduated as an Electronics and Communication Engineer in 2005, from Jawaharlal Nehru Technological University, Hyderabad, India, and received the Master of Technology degree in 2009 from the JNTU College of Engineering (Autonomous), Hyderabad, India. In 2012 he joined as an Associate Professor in the Department of Electronics Communication Engineering in Lords Institute of Engineering and Technology, Hyderabad and currently is the Head of Department E&CE. His areas of interestare Wireless & Mobile Communications, ADHOC Wireless Networks and Digital Signal processing.