I. INTRODUCTION

Asynchronous serial Communication has advantages of less transmission lines, high reliability and long transmission distance. UART allows full-duplex communication in serial link, thus has been widely used in the data communications and control system. It is widely used in data exchange between Processor and peripherals. UART converts data from parallel to serial at transmitter with some extra overhead bits using shift register and vice versa at receiver. To the processor the UART appears as an 8-bit UART with status register and BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.4 and realized on FPGA. The results indicate that this model eliminates the need for higher end, expensive testers and thereby it can reduce the development time and cost.

II. BIST TECHNIQUE

VLSI testing problems like Test generation problems, input combinatorial problems, gate to I/O pin ratio problems are discussed[3] and this motivated designers to identify reliable test methods in solving these difficulties. An insertion of special test circuitry on the VLSI circuit that allows efficient test coverage is the answer to the matter.

Abstract: Asynchronous serial communication is usually implemented by Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. Lately, built-in self-test (BIST) has been of great importance in the manufacture of very large scale integration (VLSI) circuits. Most BIST schemes compress the test response into a compact signature using space and/or time compaction. A fundamental problem associated with response compaction is error masking or aliasing. In this thesis, an alternative zero-aliasing test response evaluation scheme for BIST is presented. UART allows full duplex serial communication link, and is used in data communication and control system. There is a need for realizing the UART function in a single or a very few chips. Further, design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, there is a need to ensure the data transfer is error proof. This paper targets the introduction of Built-in self test (BIST) and Status register to UART, to overcome the above two constraints of testability and data integrity. The 8-bit UART with status register and BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.4 and realized on FPGA. The results indicate that this model eliminates the need for higher end, expensive testers and thereby it can reduce the development time and cost.

Keywords: UART, BIST, Error Check, Status Register, LFSR.
This has been addressed by the need for design for testability (DFT) and hence the need for BIST. This is to specify test as one of the system functions and thus becomes self-test. BIST is an on-chip test logic that is utilized to test the functional logic of a chip, by it. With the rapid increase in the design complexity, BIST has become a major design consideration in DFT methods and is becoming increasingly important in today’s state of the art SOCs. A properly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduces maintenance cost. BIST solution consists of a Test Pattern Generator (TPG), the circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling. Fig. 1 shows a BIST module composition. Generic BIST architecture components [7] are:

**Circuit under Test (CUT):** This is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

**Test Pattern Generator (TPG):** It generates the test patterns for the CUT. It is a dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically. Normally, the pattern generator generates exhaustive input test patterns to the CUT to ensure the high fault coverage. For example, a CUT with 10 inputs will require 1024 test patterns.

**Test Response Analysis (TRA):** It analyses the value sequence on PO and compares it with the expected output.

**Fig.1. A generic BIST module.**

**BIST Controller Unit (BCU):** It controls the test execution; it manages the TPG, TRA and reconfigures the CUT and the multiplexer. It is activated by the Normal/Test signal and generates a Go/No-Go. During BIST mode, it selects input from the pattern generator to CUT while during functional mode, selects primary inputs. There are various approaches being used to generate test patterns for BIST [6], [7], viz. ROM, LFSR, binary counters, modified counters, cellular automation. A binary counter can generate an exhaustive but not randomized test sequences. Drawback of binary counters as the pattern generator is, it requires more hardware than typical Linear Feedback Shift Register (LFSR) pattern generator. Modified counters also have been successfully as test-pattern generators.

### III. PROPOSED UART ARCHITECTURE WITH BIST

The architecture proposes an 8-bit UART which operates at a baud rate of 9600 bps with a status register to monitor the correctness of every received data byte and enhance the testability of circuit by the introduction of BIST module. The hardware architecture of the 8-bit UART with Status register, incorporated with BIST module is explained in the following sections. The proposed model has two major modules viz. UART and BIST. Further in the UART, we have transmitter receiver, and baud rate generator. Baud rate generator works at 50 MHz and further reduced as required for the operations in transmitter and receiver to achieve baud rate of 9600 bps. BIST has a control register, pattern generator and a comparator, as shown in fig.2.

**Fig.2. UART with BIST architecture.**

#### A. UART Transmitter

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal (fig. 3). The baud rate generator output will be the clock for UART transmitter.

**Fig.3. UART Transmitter.**

Data is loaded from the parallel inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR (Write) input. FIFO is 16-byte register. If FIFO is full, it sends FIFO Full (FF) signal to peripheral as shown in fig. 4. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At the same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is
empty, it will send the signal to THR and it indicates that TSR is ready to receive data from THR. TSR is an 11-bit register in which framing process occurs. In frame, start bit, parity bit and one stop bit will be added as shown in fig.6. Now data is transmitted from TSR to TXOUT serially. Fig.5 is the flowchart explaining transmission of serial data from FIFO to transmitter output.

**Fig. 4. Transmitter flowchart – Input to FIFO.**

**Fig. 5. Transmitter flowchart – FIFO to TXOUT.**

**Fig.6. UART Frame Format.**

**B. UART Receiver**

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. The receiver sampling is 16 times to that of the transmitter baud rate. In the architecture of UART receiver (fig.7), initially the logic line (RxIn) is high.

**Fig.7. UART Receiver.**

**Fig.8. Receiver flowchart (Input to FIFO).**

Whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver
Shift Register (RSR) one by one where the entire frame is stored. RSR is a 12 bit shift register. Fig.8 shows the receiver logic. Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The remaining bits in the RSR are used by the error logic block. Then, if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO (Fig.9). When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7 pins.

Fig.9. Receiver flowchart (FIFO to Output).

C. BIST Pattern Generator

LFSR is used to generate pseudo-random test pattern for the BIST. A LFSR is a shift register where the input is a linear function of two or more bits (taps). It consists of D flip-flops and linear exclusive-OR (XOR) gates. The bits contained in selected positions in the shift register are combined in some sort of function and the result is fed back into the register's input bit. The selected bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift, filling the position that is emptied as a result of the shift. The bit positions selected for use in the feedback function are called "taps". The list of the taps is known as the "tap sequence". The largest state space possible for such an LFSR will be 2n-1 all possible values except the zero state.

D. BIST Operation

For BIST, UART is set in an internal loop back mode (fig. 2). This is used to test both the transmitter and receiver of the UART. This will loop-back the serial data and transmit the data back to the receiver. For the BIST, the test pattern is generated by LFSR as mentioned in the last section and the pattern is loaded to the FIFO of the UART transmitter.

IV. SIMULATION RESULTS

The verilog HDL coding and simulation of the design are done in Xilinx tool ISim 14.4. The operating clock frequency used for simulation is 50 MHz. The baud rate set is 9600bps. Data word length is 8-bits.

A. Simulation Results of Transmitter

The fig. 10 shows the serial transmission of data. Data transmitted is “10101010”. This 8-bit data is loaded to transmit shift register and start, stop & parity bits are added to form the frame inside TSR and sent to TXD.

Fig.10. Simulation result of UART transmitter.

B. Simulation Results of Receiver

The UART receiver converts the serial data into parallel Form and makes it available at RxData [7:0]. The Serial data is received at RXD pin. Each bit is sampled and the sampled bit is saved into receive shift register. From this, the frame Bits viz. start, parity and stop bits are discarded in RSR and written to receive FIFO, RxData. The 8-bit data simulated is “11111111”. Further received data will be stored in the remaining FIFO locations. Fig.11 shows the reception of serial data

Fig.11. Simulation result of UART receiver

C. Simulation Results of BIST Operation

The fig.12 shows the simulation result of BIST module. The pattern generated by LFSR is transmitted from transmitter and received in receive FIFO.
UART Realization with BIST Architecture in FPGA

The transmit FIFO is compared with the receive FIFO after the reception of each word. The comparison starts after the delay of transmitter for sending the data and receiver for reception of the data. In this simulation, the first byte sent is “00000001” which matches in both FIFO; hence the test status bit is set ‘1’.

V. CONCLUSION

The architecture of UART that support 8-bit data word length at 9600 bps baud rate for serial transmission of data with the addition of status register for detecting errors in data transfer and BIST which allows to test the circuit itself, is introduced. Working of UART has been tested using Xilinx ISE simulator, which is implemented on FPGA. With error checking status register, we can detect the different types of errors occurred during communication and hence correct them. With the implementation of BIST, expensive tester requirements and testing procedures starting from circuit or logic level to field level testing are minimized. The LFSR replaces the function of the external tester features such as a test pattern generator by automatically generating pseudo random patterns to give good fault coverage to the UART module. Although the additional BIST circuit increases the hardware overhead and design time, it eliminates the need to acquire high-end testers. The reduction of the test cost helps in the reduction of overall production cost.

VI. REFERENCES


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