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FPGA Implementation for Simulation of BPSK Modulator

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Abstract: BPSK Modulator is one of the binary modulation techniques and here using Matlab/Simulink environment and System Generator, as well as tool from Xilinx used for FPGA design we see simulation results and also we do implementation of the modulator on a Spartan 3E Starter Kit board. The modulator algorithm has been implemented on FPGA using the VHDL language on Xilinx ISE 12.3. The modulated signal obtained from simulations was compared with the signal obtained after implementation.

Keywords: BPSK Modulator, FPGA, Xilinx ISE12.3, Spartan 3E Starter Kit Board.

I. INTRODUCTION

The BPSK (Binary Phase Shift Keying) is one of the three basic binary modulation techniques. It has as a result only two phases of the carrier, at the same frequency, but separated by 180º. The general form for the BPSK signals are according to (1), where fc is the frequency of the carrier.

$$s_i(t) = \begin{cases} s_1(t) = -A\sin(2\pi f_c t), & if\ 0_T \\ s_2(t) = +A\sin(2\pi f_c t), & if\ 1_T \end{cases} \quad (1)$$

If "1" was transmitted, the modulated signal remained the same as the carrier, with 0º initial phase, but if "0" was transmitted, the modulated signal would change with 180º, like shown in fig.1. The aim of the paper is to generate BPSK modulation which is a popular modulation technique used in communication industry, thus its symbol error performance and bandwidth efficiency.

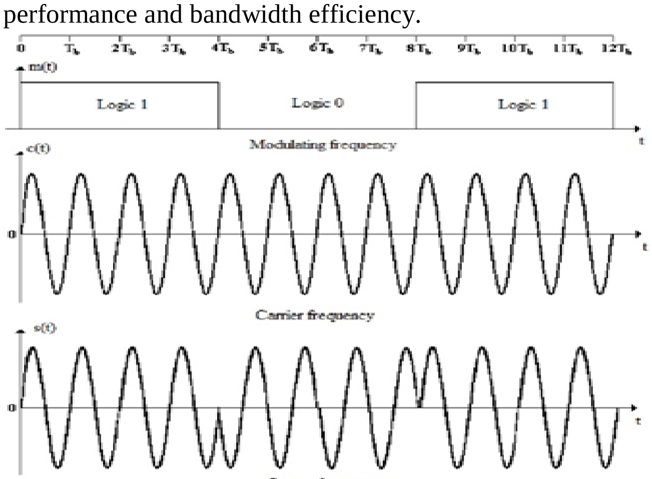

Figure1. PSK modulation.

The paper is organized into 6 sections. Introduction which represents section 1 describes the basics of the BPSK modulation. In section2, different implementations of the BPSK modulator in Simulink and System Generator are presented. In section3 we offer information about the hardware and software tools used. Section 4 is dedicated to the implementation of the modulator on the Spartan 3E Starter Kit board and section 5 to results. The final section, 6, presents conclusions and future work.

II. BPSK MODULATOR.

A. BPSK Modulator in Simulink

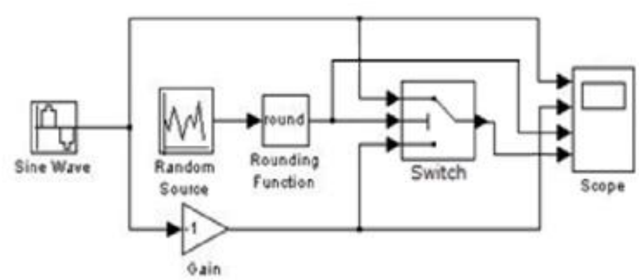

Figure2. BPSK Modulator in the Simulink environment.

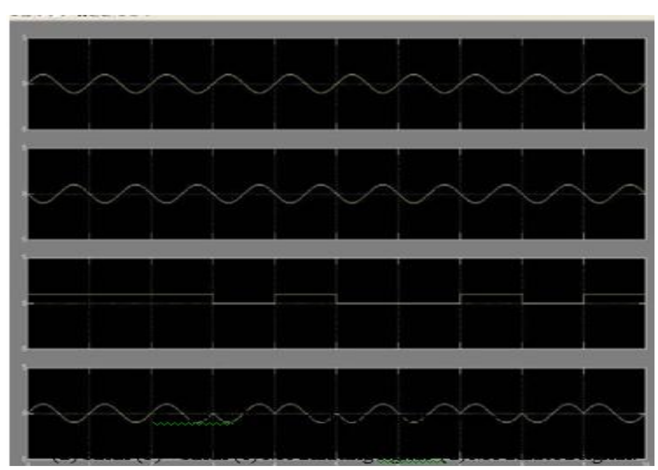

Figure3. The waveforms on the scope (a) Sinus (b) Sinus

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(c) Modulating signal (d) Modulated signal.

Fig.2 shows an implementation of a BPSK modulator in the Simulink environment and fig.3 the waveform generated by the corresponding blocks. The Simulink block set contains: the sine wave block (fig.2) which generates a sinus waveform (fig.3a) and with the help of the gain block, a sinus with phase difference of 180º (fig.3b), the blocks: random source and rounding function (fig.2) which generates the binary sequence or the modulating signal (fig.3c) and the switch (fig.2) which will choose between the first or third output depending on the value of the second input. If the second input is “1”, the output value will be sinus, but if the second input is “0”, the output will be sinus (fig.3d).

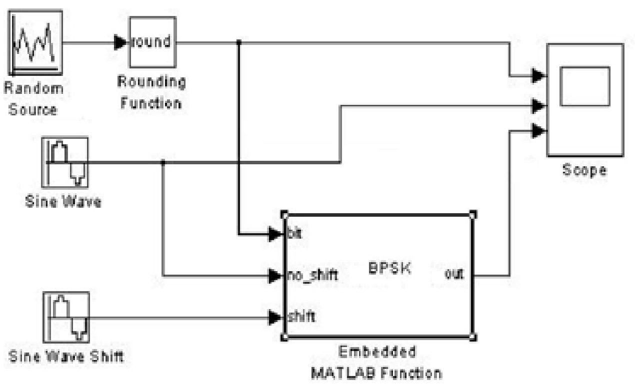

Figure4. Second implementation of the BPSK Modulator in Simulink.

TABLE I.
MATLAB CODE OF THE EMBEDDED FUNCTION

```
function out=BPSK(bit, no_shift,
shift) if bit==1
      out=no_shift;
  else out=shift;
end
```

Fig.4 represents a second implementation of the modulator in the same Simulink environment. The Simulink block set contains approximately the same blocks, the main difference been the embedded Matlab function. This block contains a Matlab language function in a Simulink model. The block accepts multiple inputs and produces multiple outputs [7]. The Matlab code of the embedded Matlab function is shown in table 1 [8].

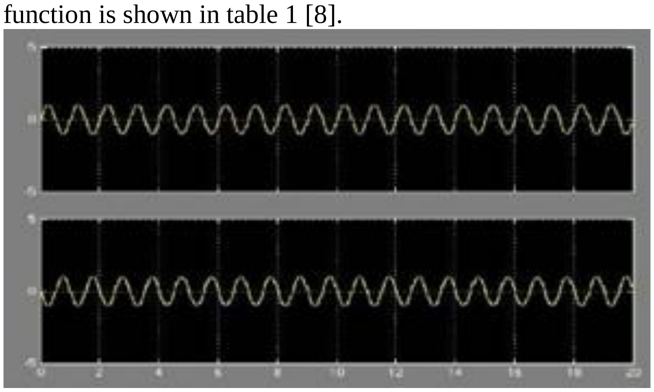

Figure5. BPSK Modulator in System Generator.

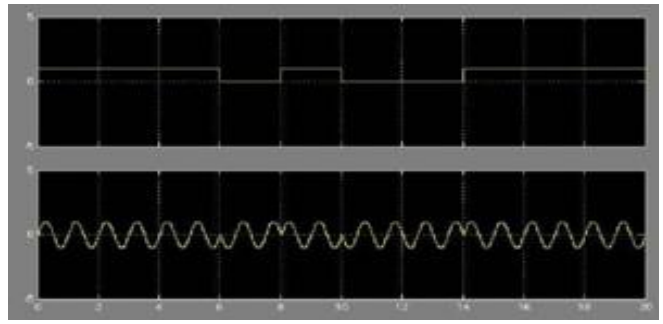

Figure 6. The modulating and modulated signals.

B. BPSK Modulator in System Generator

System Generator is a digital signal processing design tool from Xilinx, based on the Simulink environment used for FPGA design. Designs are made in the Simulink environment using a Xilinx specific blockset. All implementation steps, including synthesis, place and route are automatically performed to generate an FPGA programming file[9]. Fig.5 and fig.7 illustrate an implementation of a BPSK Modulator using System Generator tools in Simulink. In fig. 5, the carrier as well as the modulating signal is generated external and the modulated signal is created inside the board and then routed to be seen on the scope as indicated in fig.6. The Simulink Blockset contains the sine wave and gain blocks, the random source and rounding function and the scope, blocks of which we talked about. The System Generator Blockset contains: the gateway in blocks which are the inputs into the Xilinx portion of the Simulink design, the mux which implements a multiplexer and the gateway out block which is the output from the Xilinx portion of the Simulink design.

In fig.7, the carrier is generated external, but the modulating signal is generated internal by a LFSR (Linear Feedback Shift Register). Fig.8 illustrates the carrier signal, sinus and –sinus, as well as the modulating signal from the LFSR and the modulated signal obtained on the board. The Simulink Blockset contains the sine wave blocks and the scopes (fig.8). The System Generator Blockset contains: the gateway in blocks, the mux, the gateway out blocks and a LFSR.

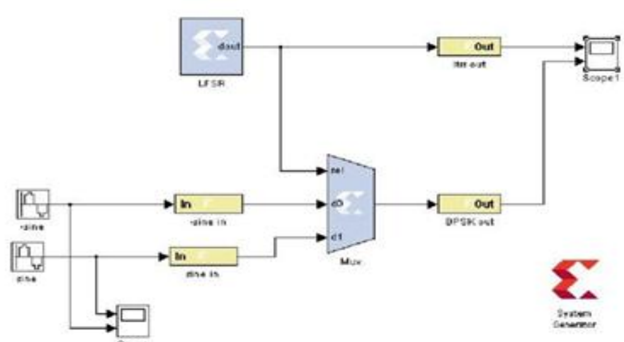

Figure7.A second implementation of the BPSK Modulator in System Generator.

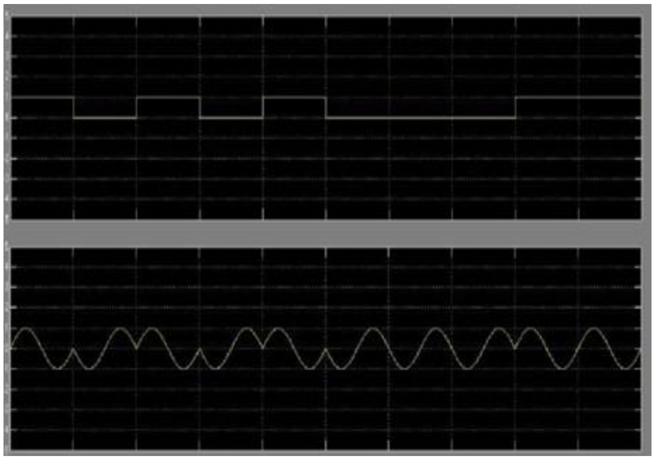

Figure8. The waveforms: (a) Sinus (b) Sinus (c) Modulating signal of the LFSR. (d)Modulated signal.

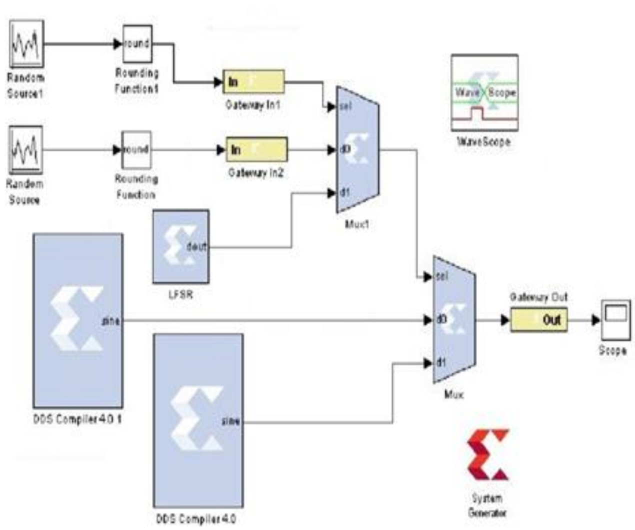

Figure9. The third model of the modulator.

The third implementation of a BPSK Modulator, illustrated in fig.9 consists of signals generated internal. The carrier is generated internal by DDS blocks from System Generator and the modulating signal can be generated internal by the LFSR or external by the Agilent 81101A Pulse Generator. Fig.10 illustrates the signals obtained after implementing the modulator. The Simulink Blockset contains the random source and rounding function and the scope, blocks of which we talked about. The System Generator Blockset contains: the gateway in blocks, the mux blocks, the gateway out block, the LFSR block and two DDS compiler blocks. The DDS Compiler Block is a direct digital synthesizer and it uses a lookup table scheme to generate sinusoids. A digital integrator generates a phase that is mapped by the lookup table into the output waveform [8]. The sinusoids can be seen in fig.10(c) and (d). The mux block implements a multiplexer. It has one select input and a configurable number of data inputs that can be defined by the user [9].

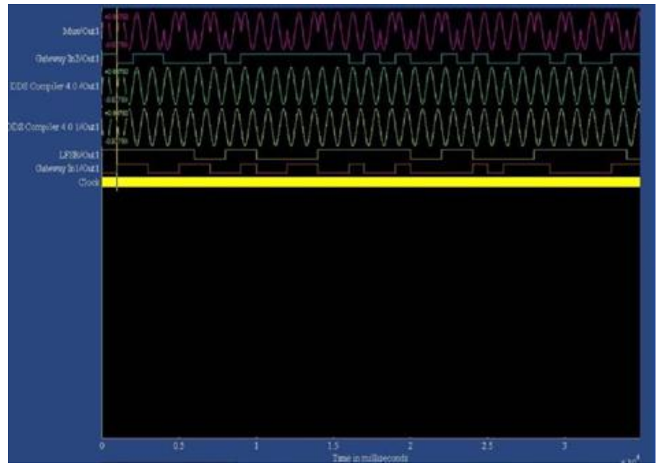

Figure10. The waveforms: The modulated signal (b) The modulating signal (c) Sinus-- Sinus (e)The output of the LFSR. The signal obtained external, from a function generator.

With the System Generator WaveScope, the user can view the waveforms generated in a design.The wavescope allows the user to observe the time-changing values of any wires in the design after the conclusion of the simulation [8]. The d0 and d1 inputs of mux1 represent the modulating signal. The sel input of mux1 selects between the d0 and d1 inputs. Because in the System Generator environment, a switch cannot be represented, we replaced it with a random sequence of bits. The same thing happens in mux2, where depending on the output of mux1, either sinus or –sinus is chosen.

III. HARDWARE AND SOFTWARE RESOURCES

The Setup Lab measurement used for realizing the BPSK modulator is illustrated in fig. 11. Some of the resources used are the Spartan 3E Starter Kit board [11], the Xilinx WebPack ISE from Xilinx, monitor, a Tektronix oscillo-scope and a pulse generator from Agilent. The Agilent

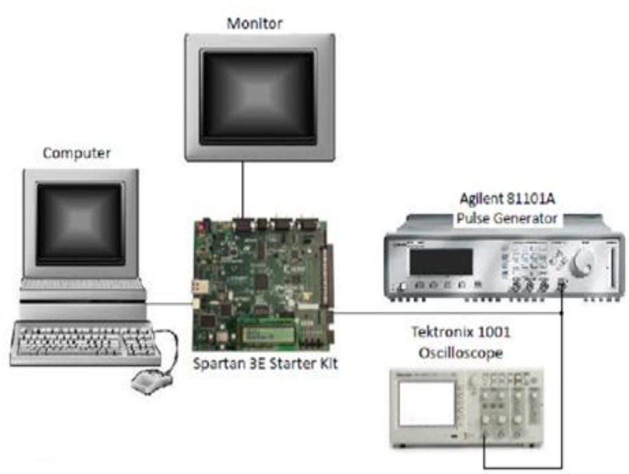

Figure11. The setup with Spartan 3E Starter Kit board

81101A is a single-channel pulse generator, capable of generating all standard pulses and bursts up to 50 MHz. The Spartan 3E FPGA Starter Kit board is a development platform based on a Xilinx Spartan 3E FPGA. It provides a development platform for embedded processing applications. The Spartan-3E family of FPGAs is designed to be well suited in a wide range of electronics applications. The ISE WebPack from Xilinx is a fully featured front-to-back FPGA design solution and it offers HDL synthesis and simulation, implementation, device fitting and JTAG programming.

IV. BPSK MODULATOR ON SPARTAN 3E STARTER KIT BOARD

The BPSK Modulator that we implemented on the Spartan 3E Starter Kit board has, as a model, the third implementation in System Generator. The carrier is generated internal, but in a ROM and that is the reason of which the sinus signal is represented discontinuous, by instantaneous samples of 16 different values [10], [11], [12]. The only thing that is different is that we used a switch that replaced the mux1 block. The switch behaves as a random sequence of bits which introduces either “1” or “0” depending on its position. Fig. 12 represents the test bench lab used in implementing the BPSK Modulator on the Spartan 3E Starter Kit Board. As explained in fig.2, the experimental setup consists of a computer, a monitor, an oscilloscope, a pulse generator and the Spartan 3E board. The ISE Web Pack runs on the computer and it programs the Spartan 3E board. The pulse generator generates the signal from fig.13 and it is measured with a LeCroy Wavesurfer Oscilloscope. The pulses are than fed to an entry of a connector on the board like illustrates in fig.14. Depending on the position of a slide switch (fig.14), the modulating signal is acquired either external, from the pulse generator or internal, from the LFSR. Opposite to System Generator, the switch can be represented or can be configured in VHDL language. The modulated signal obtained is routed to the VGA port of the board, in order to be seen on the monitor.

Figure12. Test bench lab.

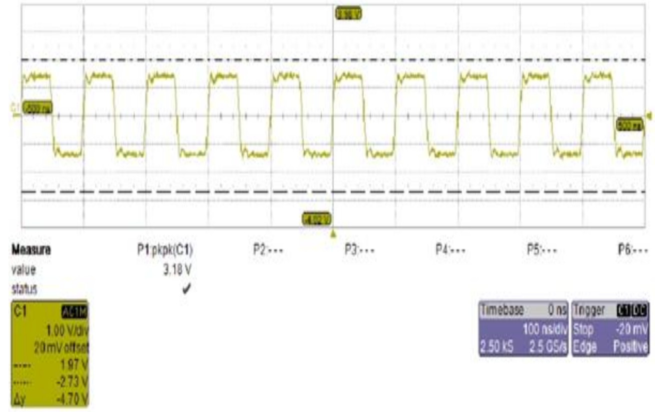

Figure13. Signal produced by the Agilent 81101A Pulse Generator.

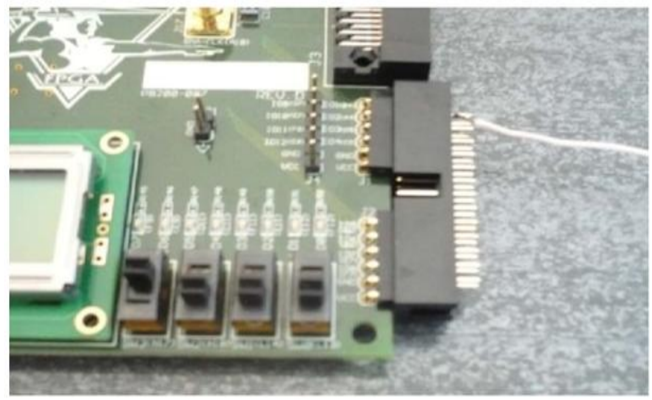

Figure14. The slide switches and the connector which makes the junction between the pulse generator and the board.

V. RESULTS

After implementing the BPSK Modulator on the Spartan 3E Starter Kit board, the signals were routed to a monitor. The BPSK modulation can be seen in fig.15 and 16. If the input data is “1”, the transmitted signal to the monitor is unchanged and has a green border on the right of the figure, but if the input data is “0”, the transmitted signal is yielded with 180º phase shift and has a red border on the right of the figure. Fig.17 represents the design summary which represents the utilization of flip-flops, LUTs, slices used from the capabilities of the FPGA from the Spartan 3E board.

Figure15. The transmitted signal if the input is 1.

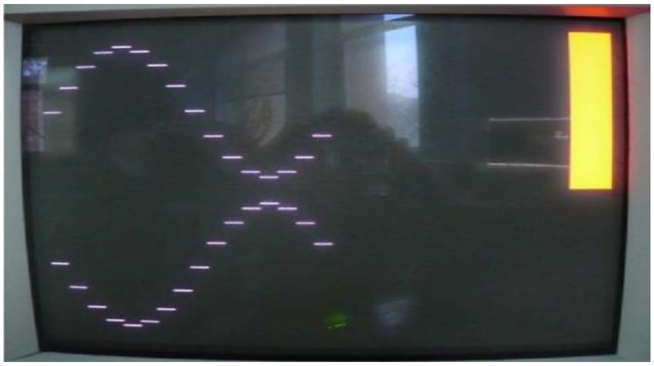

Figure16. The transmitted signal if the input is 0.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	679	9,312	7%	
Number of 4 input LUTs	952	9,312	10%	
Number of occupied Slices	765	4,656	16%	
Number of Slices containing only related logic	765	765	100%	
Number of Slices containing unrelated logic	0	765	0%	
Total Number of 4 input LUTs	1,101	9,312	11%	
Number used as logic	952			
Number used as a route-thru	149			
Number of bonded IOBs	39	232	16%	
Number of BUFGMUXs	3	24	12%	
Average Fanout of Non-Clock Nets	3.18			

Figure17. Design Summary.

VI. CONCLUSIONS AND FUTURE WORK

I conclude that we have two implementations of the BPSK Modulator in the Matlab/Simulink environment, the first with simple blocks and the second, with a block in which we wrote Matlab code. Then, we made a proposal of three implementations of a BPSK modulator in System Generator. In the first, the three signals: the carrier, the modulating and the modulated signals where generated external. In the second scheme, the carrier is generated external, and the modulating signal is generated internal by a LFSR. And in the third scheme, all three signals were generated internal with the exception of the modulating signal which can be obtained either internal by the LFSR, or external by the pulse generator. In the second part of the paper, we implemented the BPSK modulator on the Spartan 3E Starter Kit based on the third proposal of the modulator made in System. Generator. If "1" was transmitted, the modulated signal remained same as the carrier, but if "0" was transmitted, the modulated signal was yielded with a 180º phase (fig.15 and fig.16). The design has been written in the VHDL programming code by Xilinx software. Our next goal is implementing all the three proposals of the BPSK digital modulator made in System Generator on the Spartan 3E Starter Kit board. We want the modulating signal to be random, not as a train of pulses obtained from the pulse generator. We also want to route the modulated signal to a high performance oscilloscope, not to a VGA monitor in order to have more accuracy in the measurements. After implementing the BPSK modulator, we want to realize a BPSK system. The system will consist of a modulator and demodulator and the signal from the modulator to demodulator will pass through a channel affected by AWGN (Additive White Gaussian Noise). The modulated and demodulated signals will be also routed to VGA monitors, but also to oscilloscopes.

VII. REFERENCES

[1] F.Xiong, "Digital Modulation Techniques", Artech House, UK, 2000.

[2] Spartan 3E FPGA Starter Kit board. User guide. Xilinx. 2011.

[3] ISE 10.1 Quick Start Tutorial, Xilinx, 2008.

[4] Spartan-3E FPGA Family Data Sheet. Xilinx. 2008.

[5] S.T.Karris, "Introduction to Simulink with Engineering Applications", Orchard Publications, USA, 2006.

[6] J.S.Ruque, D.I.Ruiz, C.E. Carrion, "Simulation and implementation of the BPSK modulation on a FPGA Xilinx 3 xcs200-4ftp256, using Simulink and the System Generator blockset for DSP/FPGA" http://www.ece.unm.edu/ xup/docs/collaboration/BPSK_Modulator.pdf.

[7] System Generator for DSP. Getting Started Guide. Xilinx. 2008.

[8] S.O.Popescu, G.Budura, A.S.Gontean, "Review of PSK and QAM – Digital Modulation Techniques on FPGA", International Joint Conference on Computational Cybernatics and Technical Informatics (ICCC-CONTI), Romania, 2010, pp.327-332. F.Ahamed, A.Scorpino, "An educational digital communications project using FPGAs to implement a BPSK Detector", IEEE Transactions on Education, Vol.48, No.1, 2005, pp.191-197.

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