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High Speed 4X4 Bit Vedic Multiplier based on Vertical and Crosswise Methods

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Abstract: The need of high speed multiplier is increasing as the need of high speed processors are increasing. A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction. This paper presents a high speed 4x4 bit Vedic Multiplier (VM) based on Vertically & Crosswise method of Vedic mathematics, a general multiplication formulae equally applicable to all cases of multiplication. It is based on generating all partial products and their sum in one step. The coding is done in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) while the synthesis and simulation is done using EDA (Electronic Design Automation) tool - XilinxISE12.1i. The combinational path delay of 4x4 bit Vedic multiplier obtained after synthesis is compared with normal multipliers and found that the proposed Vedic multiplier circuit seems to have better performance in terms of speed.

Keywords: Vedic Multiplication, Urdhva Tiryakbhyam Sutra, Ripple Carry Adder..

I. INTRODUCTION

Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [2]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors.

This paper describes the design and implementation of 4x4 bit Vedic multiplier based on Urdhva-Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA (Electronic Design Automation) tool. The paper is organized as follows. Section 2 describes the Vedic Mathematics. Section 3 describes the Design of Vedic Multiplier. Section 4 illustrates the implementation and result of Vedic multiplier module so obtained while Section 5 comprises of Conclusion. Section 6 comprises of References.

II. VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic math's deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful.

The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.

2. Chalana-Kalanabyham– Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous one.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or non completion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charamena – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, and area and power consumption.

The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

III. DESIGN OF VEDIC MULTIPLIER

A. Urdhva – Triyagbhyam (Vertically and Crosswise)

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498×2314). The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig.1. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

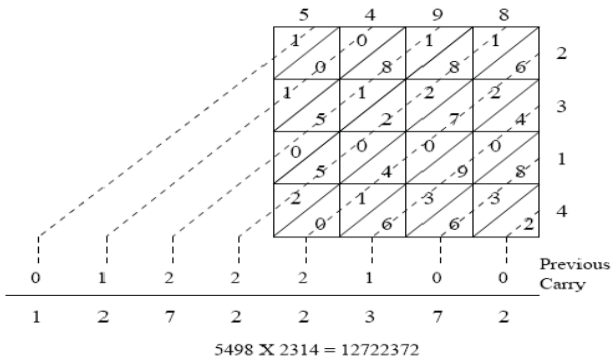

Fig.1. Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

The design starts first with Multiplier design that is 2x2 bit multiplier as shown in fig.2. Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products.

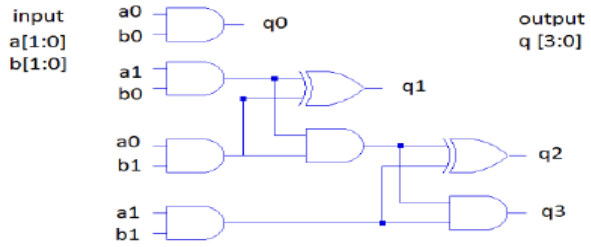

Fig.2. Hardware Realization of 2x2 block

To scale the multiplier further, Karatsuba–Of man algorithm can be employed. Karatsuba-Ofman algorithm is considered as one of the fastest ways to multiply long integers. It is based on the divide and conquers strategy. A multiplication of 2n digit integer is reduced to two n digit multiplications, one (n+1) digit multiplication, two n digit subtractions, two left shift operations, two n digit additions and two 2n digit additions.

The algorithm can be explained as follows:

Let X and Y are the binary representation of two long integers:

$$X = \sum_{i=0}^{k-1} x_i\, 2^i$$

$$Y = \sum_{i=0}^{k-1} y_i\, 2^i$$

We wish to compute the product XY. Using the divide and conquer strategy, the operands X and Y can be decomposed into equal size parts XH and XL, YH and YL, where subscripts H and L represent high and low order bits of X and Y respectively.

Let k= 2n. If k is odd, it can be right padded with a zero

$$X = 2^n \sum_{i=0}^{n-1} x_{i+n} 2^i + \sum_{i=0}^{n-1} x_i\, 2^i = X_H\, 2^n + X_L$$

$$Y = 2^n \sum_{i=0}^{n-1} y_{i+n} 2^i + \sum_{i=0}^{n-1} y_i\, 2^i = Y_H\, 2^n + Y_L$$

The product XY can be computed as follows:

$$P = X * Y$$
$$= (X_H 2^n + X_L)(Y_H 2^n + Y_L)$$
$$= 2^{2n}(X_H * Y_H) + 2^n\big((X_H * Y_L) + (X_L * Y_H)\big) + (X_L * Y_L)$$

For Multiplier, first the basic blocks, that are the 2x2 bit multipliers have been made and then, using these blocks, 4x4 block has been made by adding the partial products using carry save adders and then using this 4x4 block, 8x8 bit block, 16x16 bit block and then finally 32x32 bit Multiplier as shown in figure 3 has been made.

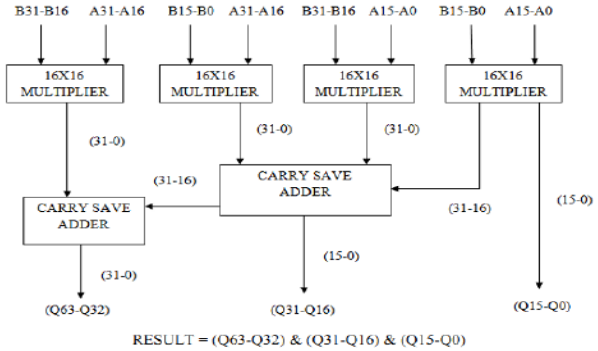

Fig.3. 32X32 Bits proposed Vedic Multiplier

IV. IMPLEMENTATION & RESULTS

In this work, 4x4 bit VM (Vedic multiplier) using "Urdhva Tiryakbhyam" Sutra is implemented in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language). Logic synthesis and simulation was done using EDA(Electronic Design Automation) tool in XilinxISE12.1i - Project Navigator and I-Sim simulator integrated in the Xilinx package respectively. Table 1 displays the comparison of synthesis results of the proposed Vedic multiplier with the Conventional multipliers in terms of time delay (in nanoseconds). The combinational path delay obtained for the proposed 4x4 bit Vedic multiplier is 13.102 ns whereas the results of 4x4 bit Array and Booth multipliers have been taken. The performance is evaluated on the Xilinx device family Spartan3, package tq144 and speed grade -5.

Table 1: Comparison of Multipliers (in nanosecond)

Device: Spartan xc3s50a-5tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
4x4 bit VM	32.001 ns	16.276 ns	13.102 ns

The RTL (Register Transfer Level) schematic of the 4x4 bit Vedic multiplier comprises of four 2x2 bit Vedic multiplier (vedic_multi_struct) v1, v2, v3, v4 and three 4-bit Ripple Carry Adder (rc_adder) v5, v6, v7 as shown in Fig.4 while the simulation results obtained are shown in Fig.5 for verification. In behavioral simulation we have tested for input bits: - "0100" (in decimal number system 4) and "0100" (decimal number system 4) as inputs and we get output as "00001000" (decimal number system 8). The inputs of 4-bits are decomposed into the input of 2-bits. The input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplicand are kh=01 and kl=00, while the input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplier are lh=00 and ll=01. Finally, the output1=00010000, indicates the final 8-bit result. However the rest signals indicate the intermediate results like partial products (sum & carry).

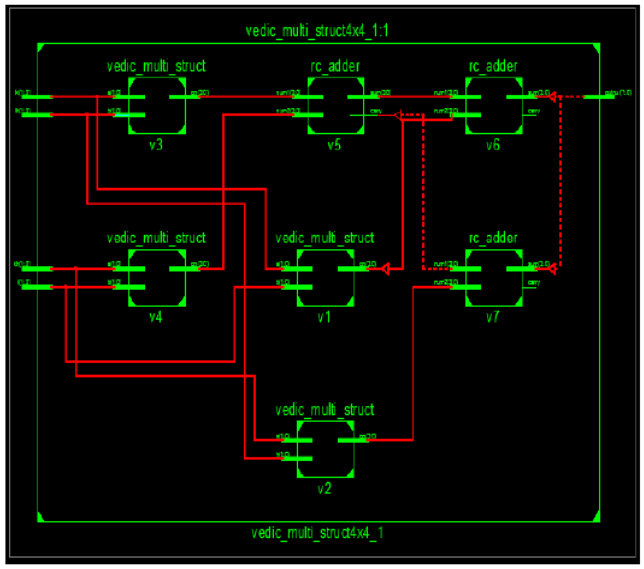

Fig.4. RTL schematic of 4x4 bit Vedic Multiplier

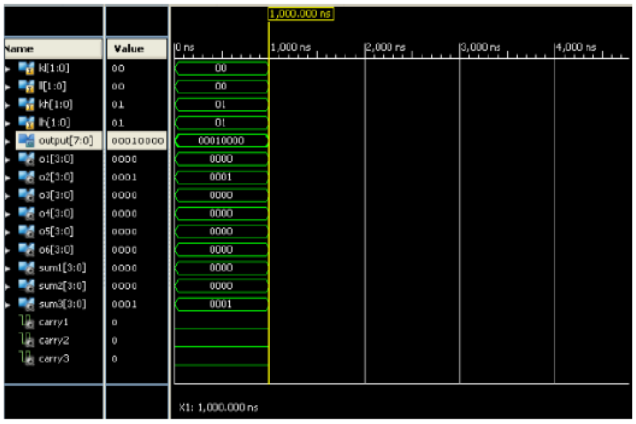

Fig.5. Simulation Result of 4x4 bit Vedic Multiplier

V. CONCLUSION

This paper presents a new method of multiplication "Urdhva Tiryakbhyam" Sutra based on Vedic Mathematics. The design of the proposed 4x4 bit Vedic multiplier is implemented on Spartan xc3s50a-5-tq144 device. The computational path delay of the Vedic multiplier is found to be 13.102 ns. Hence it can be concluded that the performance of the proposed 4x4 bit Vedic multiplier seems to be highly efficient in terms of speed when compared to Conventional multipliers. Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose. The idea proposed here may set path for future research in this direction.

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