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Ultralow Power High Speed 4-2 Compressor Design for Sub Threshold Voltage Logics with 45nm Technology

JEEVAN KUMAR NEELA[1], DR. S.P. VENU MADHAVA RAO[2]

[1]PG Scholar, Dept of ECE(DSCE), Sreenidhi Institute of Science & Technology, Hyderabad, TS, India,
E-mail: Jeevankumar.neela@gmail.com.

[2]Professor & HOD, Dept of ECE, Sreenidhi Institute of Science & Technology, Hyderabad, TS, India.

Abstract: 4-2 compressors are the most popular bit-compressing cells with principal application in multi-operand addition and multiplication hardware. Therefore, performance of 4-2 compressor is particularly influential in the efficiency of multiplication intensive computations. Realization of these compressing cells is mainly based on XOR/XNOR gates, which are functionally equivalent to three simpler ones among AND/NAND and OR/NOR gates. Decomposition of XOR/XNOR gates in some 4-2 compressors to their constituent simpler ones may lead to removal of some hardware redundancy. A low-power high speed 4-2 compressor circuit is implemented for fast digital arithmetic integrated circuits, which has been widely employed for multiplier realizations. The implementation of circuit for the XOR–XNOR module for sub threshold logics at 45nm technology using Cadence described in this paper eliminates the weak logic on the internal nodes of pass transistors with a pair of feedback NMOS–PMOS transistors. Driving capability has been considered in the design as well as in the simulation setup so that these 4-2 compressor cells can operate reliably in any tree structured parallel multiplier at very low supply voltages. The implemented 4-2 compressor, as such, and those of reference works will be simulate and then Sub threshold Logic voltages (0.3V-0.9V) have to provide on CADANCE tool at 45nm Technology. The Implemented circuit shows power consumption improvement, Maximum output delay of the circuit presents greater improvement. Power consumption, delay and PDP of implemented 4-2 compressor circuit had been compared with earlier reported circuits and implemented circuit is proven to have the minimum power consumption and the lowest delay.

Keywords: XOR/XNOR Module, Differential Multiplexer Module, Power Consumption, Delay, Sub Threshold Voltage Logics, Cadence, Gpdk045.

I. INTRODUCTION

Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing systems, such as computer graphics, scientific calculation, and image processing and so on. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. The multiplier architecture consists of a partial product generation stage, partial product reduction stage and the final addition stage. The partial product reduction stage is responsible for a significant portion of the total multiplication delay, power and area. Therefore in order to accumulate partial products, compressors usually implement this stage because they contribute to the reduction of the partial products and also contribute to reduce the critical path which is important to maintain the circuit's performance [1]. This is accomplished by the use of 3-2, 4-2, 5-2 compressor structures. A 3-2 compressor circuit is also known as full adder cell [2]. As these compressors are used repeatedly in larger systems, the improved design will contribute a lot towards overall system performance. The internal structure of compressors is basically composed of XOR-XNOR gates and multiplexers. The XOR-XNOR circuits are also building blocks in various circuits like arithmetic circuits, multipliers, compressors, parity checkers, etc. Optimized design of these XOR-XNOR gates can improve the performance of multiplier circuit [3]-[7]. In present work, a new 4-2 compressor has been implemented using XOR-XNOR and differential MUX modules. Use Implemented circuit in partial product accumulation reduces transistor count as well as power consumption. This paper is organized as follows: In section II building blocks of compressor circuit are described and a XOR-XNOR and MUX circuits have been implemented in 45 nm Technology as well as at Sub threshold logic voltages. In section III A 4-2 compressor has been designed with XOR-XNOR and MUX modules at 45nm Technology as well as at Sub threshold logic voltages. Section IV Use of Implemented circuit in partial product accumulation of 8X8-MULTIPLIER. Section V Discuss the results. Finally section VI concludes the work.

II. BUILDING BLOCKS 4-2 COMPRESSOR

A. Implementation of XOR-XNOR module:

There are different architectures and designs of 4-2 compressor circuits reported in literature. These are mainly composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX). Complementary CMOS uses the dual networks to implement a given function. One part consists of complementary pull-up PMOS network while other part consists of pull-down NMOS networks. This technique requires more numbers of transistors and large layout area. As shown in Fig. 2.1 the implemented XOR-XNOR module had two pull-up PMOS-transistors and two pull-down NMOS–transistors are added to restore full swing operation. The circuit performs successfully at low supply voltages but this comes at the expense of increased area and number of transistors. Another disadvantage of the circuit is that each of the inputs drives four gates instead of two gates doubling the input load. This will cause slow response when this circuit is cascaded.

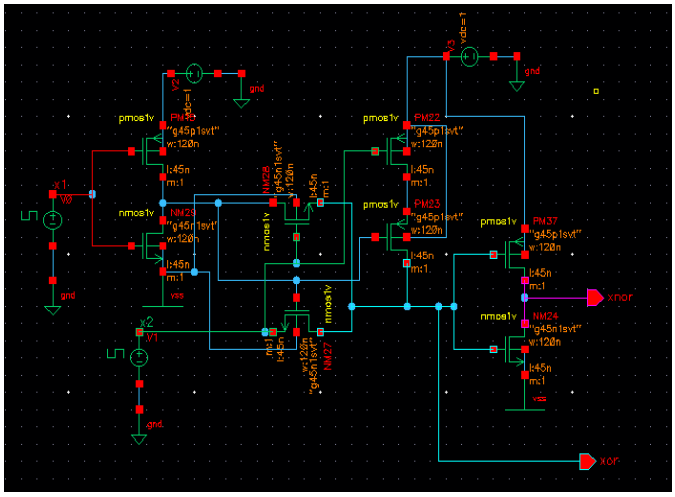

Fig.1. Implemented Design of XOR-XNOR.

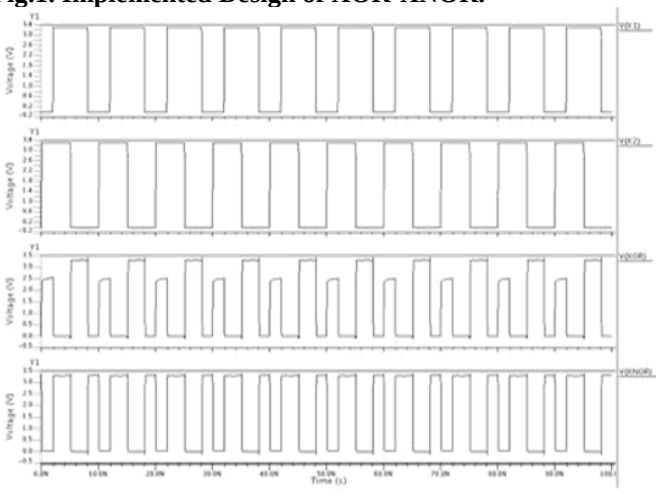

Fig.2. Input and output waveform for XOR-XNOR.

B. Implementation of Multiplexer Module

Multiplexer module produces an output that accurate reflects state of one of the number of data inputs, based on value of one or more control inputs. Two data inputs multiplexer is named as 2-1 Multiplexer. The carry generator module in compressor produces the signals generated by multiplexer. As shown in the fig.2.2 the implemented Multiplexer with 6 transistors for sub threshold logics at 45nm technology is used in low power Compressor cells. When buffers are not used at the output, this design of the multiplexer is faster than the CMOS design. As shown in the Fig.3.1 the 4-2 compressor circuit has 5 inputs and 3 outputs.

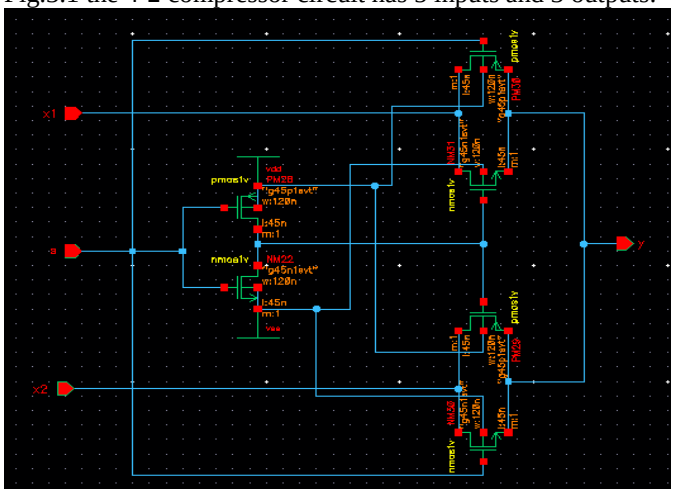

Fig.3 Implemented Design of MUX.

III. IMPLEMENTATION OF 4-2 COMPRESSOR

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two cascaded 3-2 compressor circuits. The present Implementation of 4-2 Compressor is build of High speed and low power XOR-XNOR and MUX modules as implemented in the previous section. The basic block diagram of 4-2 Compressor is as follows.

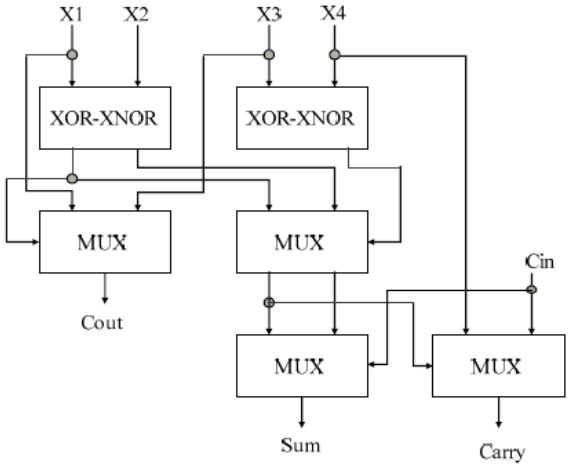

Fig.4. Basic Block Diagram of 4-2 Compressor.

As shown in the Fig.4 the 4-2 compressor circuit has 5 inputs and 3 outputs.

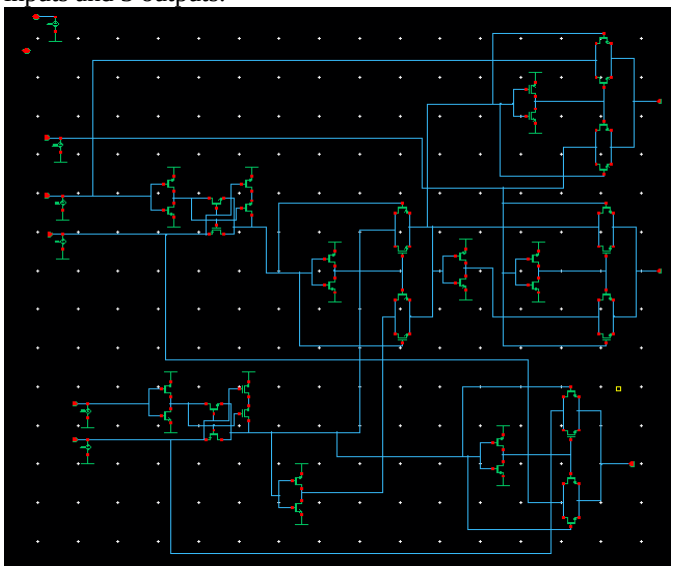

Fig.5. Implemented Design of 4-2 Compressor.

The 4-2 compressor has five inputs and three outputs, where the four inputs X1, X2, X3, X4 and the output Sum have the same weight. On the other hand, the outputs Carry and C-out have one bit order higher, thus presents a higher compression ratio and a more regular interconnection arrangement. One vital point to be emphasized in this compressor is the independent of the input carry C-in in the output carry C-out. The 4-2 compressor optimized at gate level with XOR-XNOR modules and carry generators by 2:1 multiplexers (MUX) reduces the critical path delay as shown in Fig.3.2. The multiplexer block at the SUM output takes the select bit prior to the inputs obtain and thus the transistors are already switched by the time they come. This minimizes the delay to a significant level.

The output of implemented 4-2 compressor based on a modified set of equations for the sum and carry outputs of the compressor as follows

$$S = X1 \oplus X2 \oplus X3 \oplus X4 \oplus C\text{-in} \quad (1)$$

$$C = (X1 \oplus X2 \oplus X3 \oplus X4)\, C\text{-in} + (X1 \oplus X2 \oplus X3 \oplus X4)' X4. \quad (2)$$

$$C\text{-out} = (X1 \oplus X2)\, X3 + (X1 \oplus X2)' X1. \quad (3)$$

IV. USE OF IMPLEMENTED CIRCUIT IN PARTIAL PRODUCT REDUCTION STAGE OF 8X8-MULTIPLIER

A. 8X8 Multiplier Using 4-2 Compressor

The multiplier architecture consists of a partial product generation process, partial product reduction process and the final addition process. The partial product reduction process is responsible for a significant portion of the total multiplication delay. For NXN multipliers partial product reduction is predetermined by stage heights. In 8X8 Multiplier maximum height of partial products at the generation stage i.e. stage-1 of reduction process is 8 bits.

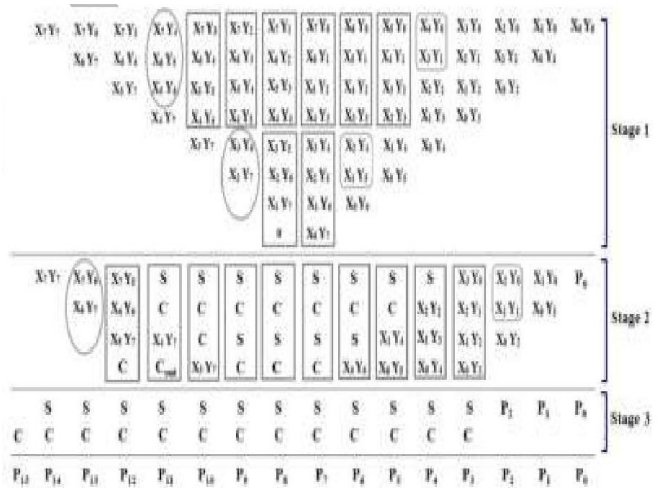

Fig.6. Partial Product Reduction Stages of 8X8 Multiplier.

The stage heights are Stage 2 = 2^m, Stage 3 = 2^{m-1}, Stage 4 = 2^{m-2}... until final stage height is 2. This format is performed with usage of 4-2 compressors (in Figure 3) while maintaining stage height. The 8x8 multiplier with the proposed scheme is shown in Figure 7. The maximum height of partial products stage (Stage 1) is 8 bits. The nearest 2^m integer smaller than 8(2^3) is 4 i.e., 2 $^{(2-0)}$. So, the height of Stage 2 should be 4 bits, which is maximum column (C) height. Examine each column (C) and the reduction is as follows,

Step 1: C1 to C4 have height less than or equal to 4 bits. So, no need to change these columns.
Step 2: C5 has 5 bits and to reduce it to 4 bits, a half adder is required.
Step 3: C6 has 6 bits and a carry bit from C5. A 4-2 Compressor is required to make its height 4 bits.
Step 4: C7 has 7 bits and a carry from C6. A 4-2 Compressor and half adder are needed to reduce it to 4 bits.
Step 5: C8 has 8 bits and 2 carry bits from C7, and so two 4-2 Compressors are required.
Step 6: C9 has 7 bits and 2 carry bits from C8. So, two 4-2 Compressors are needed with one of its input as 0.
Step 7: C10 has 6 bits, 2 carries and C-out from C9. A 4-2 compressor and full adder are needed to reduce it to 4 bits.
Step 8: C11 has 5 bits and 2 carries from C10. So, one 4-2 compressor is required.
Step 9: C12 has 4 bits and a carry, C-out form C11. So, a full adder is required, after which each column has less than or equal to 4 bits.

Next stage height is to be 2^{2-1} = 2 which is last stage. The reduction steps to have maximum column height 2 are
Step 1: C1, C2 needs no changes in them, but C3 has 3 bits. So, a half adder is required to reduce to 2 bits.
Step 2: C4 has 4 bits and carry from C3. Thus, a 4-2 compressor is needed.
Step 3: C5 to C13 has 5 bits including a carry from just preceding columns. So, a 4-2 compressor is required.
Step 4: C14 has 2 bits and a carry, C-out from C13. So, a full adder is required to reduce it 2 bits.

Now, after this stage each column has less than or equal to 2 bits, after which the reduction phase is completed and this last stage is given to Carry Propagate Adder for producing the final multiplier result. This 8x8 multiplier uses 18 no. of 4-2 Compressors, 16 full adders and 4 half adders. Thus the performance of 4-2 Compressor has been increased performance of Multiplier will be increase.

V. RESULTS AND DISCUSSIONS

The Input-Output waveforms of the Implemented 4-2 Compressor circuit with the power consumption signal are as follows. The four inputs X1, X2, X3, X4 which have to compress a carry input signal C-in and the output signals Sum have the same weight. On the other hand, the outputs Carry and C-out have one bit order higher. And the power signal (:pwr) is also shown in the output waveforms.

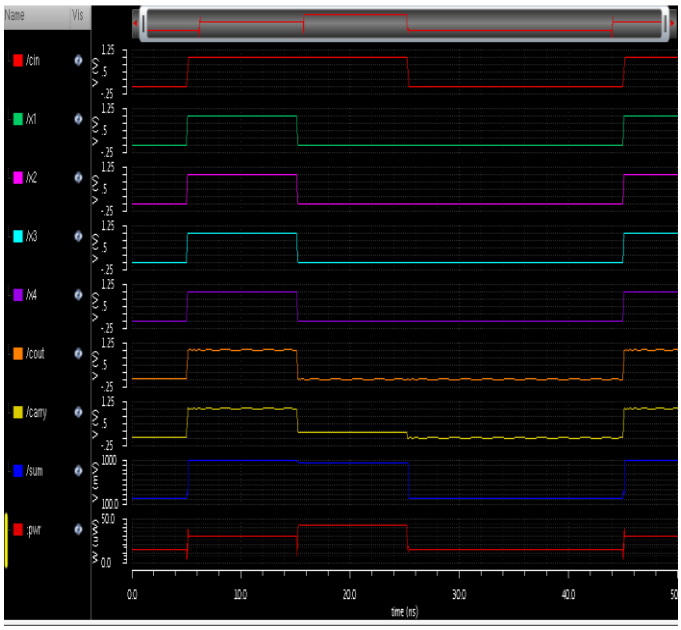

Fig.7. Input Output waveforms of 4-2 Compressor.

In this work an improved 4-2 compressor circuit has been designed with new XOR-XNOR module and 2:1 multiplexer in 45nm CMOS technology using Cadence Tool. Thus the powerConsumption of 4-2 Compressor significantly decreases because of Sub Threshold logic voltages of 0.3V to 0.9V.

Table.1. Power and delay of 4-2 Compressor circuit

Supply voltage (V)	Power consumption (pW)	Output Delay (pS)	PDP (10^{-24}J) yJ
0.3	178.4	69	12309.6
0.6	306.9	46	14117.4
0.9	507.4	37	18773.8

Power Consumption of Implemented 4-2 Compressor circuit has been varying from 30.09pW to 94.87pW and Delay of the circuit has been varying from 64pS to 13pS with varies Supply voltage of 0.3V to 0.9V.

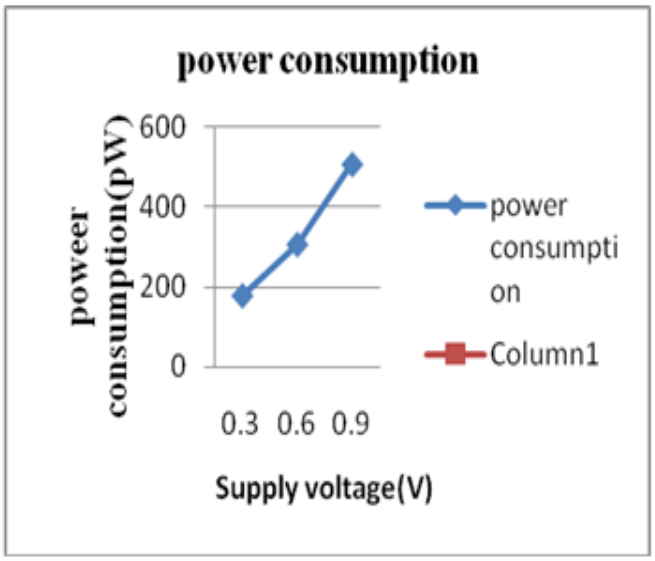

Fig.8. Power consumption of 4-2 compressor circuit.

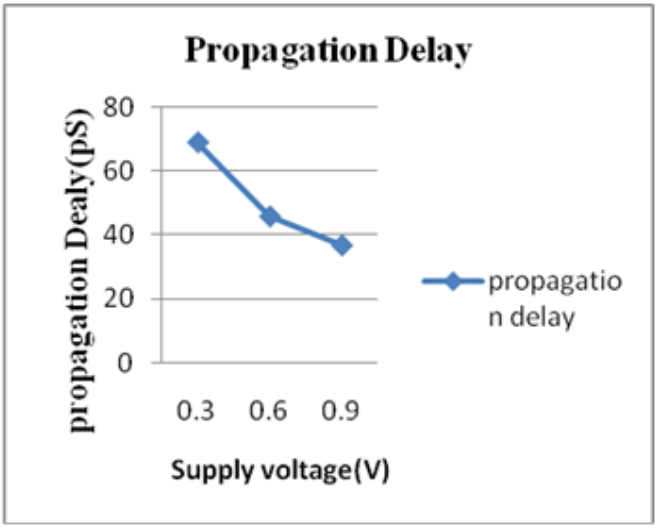

Fig.9. Propagation delay of 4-2 compressor circuit.

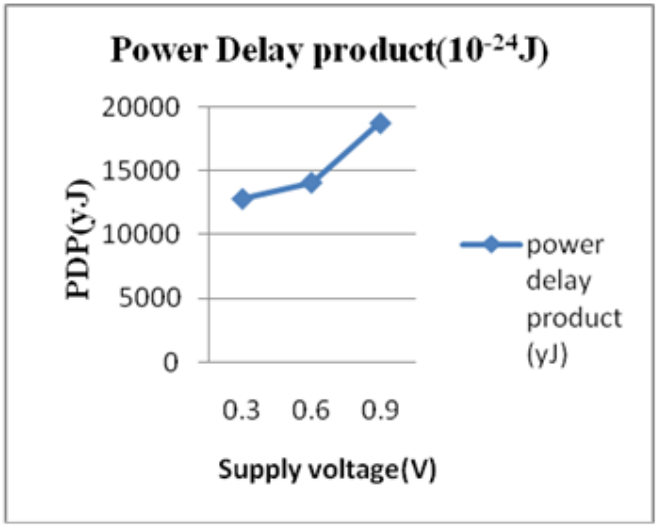

Fig.10. Power Delay product of 4-2 compressor circuit.

Fig7 shows the power consumption variation of 4-2 Compressor circuit with variation in supply voltage. Power consumption of circuit is increasing with rise in supply voltage from 0.3V. Fig9 shows the Propagation delay of 4-2 compressor circuit decreases with increase in supply voltage. Fig10 shows the Power Delay product of 4-2 compressor circuit in YOCTO Joules(10^{-24}). Implemented 4-2 compressor uses 40 transistors and also works with supply voltage less than 1V. Table.2 shows the comparison of the previous implementations of 4-2 compressor and as a result the 4-2 Compressor Implemented in this paper has the good performance over all the previous Implementations.

Table.2. Comparison of 4-2 Compressor performance

Compressor circuits	Max. Power consumption (pW)	Max. Output Delay (pS)	PDP (10^{-22}J)
Ref.[15] (180nm)	**3830.90**	**57.24**	**2192.80**
Ref.[16] (180nm)	**3821.60**	**72.84**	**2783.65**
Ref. [10]	**3357.40**	**27.74**	**931.342**
Implemented with 45nm	**507.4**	**37**	**187.738**

VI.CONCLUSION

A 4-2 compressor circuit based on XOR-XNOR and MUX modules has been implemented at 45nm Technology for Sub threshold voltage logics Using Cadence Tool which provide better performance. The implemented design shows the lowest power consumption of Pico watts with supply voltage of 0.3V. The implemented design provides maximum output delay of 72pS at 0.3V. Further, circuit shows PDP of 12309.6×10^{-24} (J) at 0.3 V. The performance of this circuit have been compared to earlier reported circuits in terms of power consumption, maximum output delay and power delay product (PDP). The proposed circuit result shows better performance than existing circuits in all aspect.

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