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Design of High Speed and Low Power ALU using Vedic Mathematics

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Abstract: The main objective of this project is to design efficient ALU using Vedic sutras. Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed ALU using Vedic sutras. A high speed processor depends greatly on the multiplier, adder, subtract or as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic Mathematics has a unique technique of calculations based on 16 Sutras. This Indian ancient Vedic mathematics rules can be combined with many advanced techniques provides lot of applications with more advantages.

Keywords: Vedic Mathematics, Multiplier, Urdhvatiryagbhyam, Pass Transistor, Probability, Carry Save Addition, Computer Algebra System, Black-Boxes.

I. INTRODUCTION

Multiplication is a complex arithmetic operation, which is reflected in its relatively high signal propagation delay, high power dissipation, and large area requirement. When choosing a multiplier for a digital system, the bit width of the multiplier is required to be at least as wide as the largest operand of the applications that are to be executed on that digital system. THE digital multiplier is a ubiquitous arithmetic unit in microprocessors, digital signal processors, and emerging media processors [1]–[4]. It is also a kernel operator in application specific data path of video and audio codecs, digital filters, computer graphics, and embedded systems [5]–[8]. Com- pared with many other arithmetic operations, multiplication is time-consuming and power hungry. The critical paths dominated by digital multipliers often impose a speed limit on the entire design. Hence, VLSI design of high-speed multipliers, with low energy dissipation, is still a popular research subject. Now a day's all CPU units, any machinery parts utilizes a basic arithmetic operations like addition, subtraction, multiplications. Each and every operation involves multiplier operation in its salvation. While there have been a lot of work on simple schemes for operand guarding, work that simultaneously considers multiplication throughput is more scarce.

Achieving double throughput for a multiplier is not as straightforward as, for example, in an adder, where the carry chain can be cut at the appropriate place to achieve narrow-width additions. It is of course possible to use several multipliers, where at least two have narrow bit width, and let them share the same routing, as in the work of Loh, but such a scheme has several drawbacks: i) The total area of the multipliers would increase, since several multiplier units are used. ii) The use of several multipliers increases the fanout of the signals that drive the inputs of the multipliers. Higher fanout means longer delays and/or higher power dissipation. iii) There would be a need for multiplexers that connect the active multiplier(s) to the result route. These multiplexers would be in the critical path, increasing whole latency as well as power consumption.

II. VEDIC MATHEMATICS

To obtain a historical perspective on Vedic Mathematics, briefly we discuss the mathematical developments in India (Boyer, 1968; Katz, 1992). Archeological excavations documented an old and highly cultured civilization in India during the third millenium B.C.E., but no Indian mathematical documents where found from that period. India like Egypt had its geometrical measurement in the form of a body of knowledge known as the Sulvasutras ("rules of the cords"). The word sutra ("thread of knowledge") means rules expressed by aphorisms relating to rituals or science. This primitive account, dating perhaps before the time of Pythagoras (6^{th} century B.C.E.), contained rules for the construction of right angles by means of triple cords. The period of the Sulvasutras was followed by the age of the Siddhantas ("systems of astronomy") starting around 500 C.E., which contributed to trigonometry the notion of the sine, namely the ratio of half a chord of a circle and half the corresponding central angle. The trigonometry of the sine function is one of the noted contributions of India to modern mathematics. Another marked development is our system of numeration for integers, called the Hindu-Arabic system (about 700 C. E.). The use of the zero symbol in India existed from the ninth century. Other developments from the same period were indeterminate analysis (Brahmagupta) and algebraic techniques. In the first centuries of the second

millenium spherical trigonometry and Pell equations (Bhaskara) were developed.

The discovery of power series for trigonometric functions took place around 1500. Hindu mathematians were inclined to further develop topics in number theory and indeterminate analysis in particular. However, these aspects did not contribute to later developments in modern mathematics such as analytic geometry, calculus, and algebra. The term vedic mathematics refers to a set of sixteen mathematical sutras and their corollaries derived from the vedas. The vedas are ancient texts written in sanskrit; the word veda means "knowledge" – knowledge both within and among the senses. it is conjectured that the vedic mathematical system was part of the sulvasutras. This is a system of calculations based on easy-to-follow rules and principles that can be used effectively to solve problems in arithmetic, algebra, geometry, and trigonometry. The vedic system was rediscovered between 1911 and 1918 by sri swami bharati krisna tirthaji and has been re-structured for use in schools. it is being taught in some schools in several countries as well as being used for scientific applications (see references to web sites).

III. TWO VEDIC METHODS

Several Vedic methods were studied during the course. Here we describe two methods, each of which is used for multiplication of two natural numbers. The workshop described later included the use of these methods. For each method we describe its goal, rules of use, correctness justification, the matching algorithmic problem, and its solution. The description of both methods uses the symbol '|' to separate the prefix and the suffix of a number. The term length of a number indicates the number of its digits.

A. Method 1

Multiplication of two numbers x (the multiplicand) and y (the multiplier), where the multiplier's digits consist entirely of nines; using the Ekanyunena Purvena sutra, which means: "By One Less Than the One Before". According to this method, the result of $x*y$ comprises two parts: a prefix and a suffix.

Case I: if the number of digits of x (x's length) is greater or equal to the number of digits of y (y's length), then: The prefix of $x*y$ is x - 1 and the suffix is y - (x - 1). The matching algorithmic problem for this method is as follows: write a function that implements the Vedic method and multiplies two natural numbers x and y, whereas y's digits consist entirely of nines. For a suitable algorithm we used the pre-defined Derive function 'FLOOR', in order to translate the Vedic instruction: "divide the number with '|' to prefix and suffix". The function FLOOR(a,b) return the quotient of the operation a/b, for example, FLOOR(758,100) = 7. The distinction between the two cases in the method, based on the length of the two multipliers, was translated to the equivalent two cases, $x \leq y$ and $x > y$. The cases are equivalent because y's digits consist entirely of nines, and therefore any number whose number of digits is equal, smaller, or greater than y would be smaller, equal or greater than y, respectively.

ALU: In digital electronics, an arithmetic logic unit (ALU) is a digital circuit that performs integer arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs. An ALU must process numbers using the same formats as the rest of the digital circuit. The format of modern processors is almost always the two's complement binary number representation. Early computers used a wide variety of number systems, including ones' complement, two's complement, sign-magnitude format, and even true decimal systems, with various[NB 2] representation of the digits. The ones' complement and two's complement number systems allow for subtraction to be accomplished by adding the negative of a number in a very simple way which negates the need for specialized circuits to do subtraction; however, calculating the negative in two's complement requires adding a one to the low order bit and propagating the carry. An alternative way to do two's complement subtraction of A−B is to present a one to the carry input of the adder and use ¬B rather than B as the second input. The arithmetic, logic and shift circuits introduced in previous sections can be combined into one ALU with common selection.

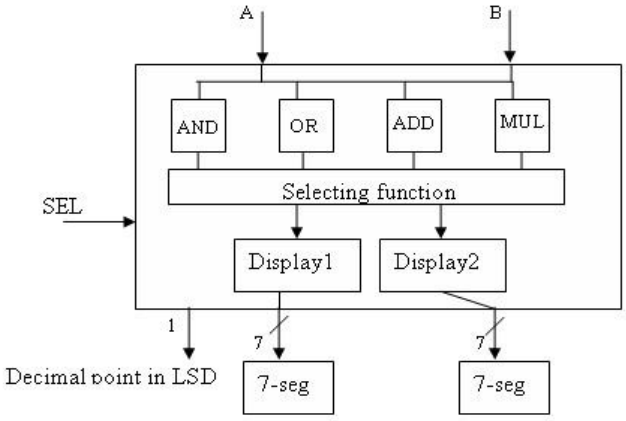

Fig.1.

B. Logical Module

In computer storage, a logical unit number, or LUN, is a number used to identify a logical unit, which is a device addressed by the SCSI protocol or Storage Area Network protocols which encapsulate SCSI, such as Fibre Channel or iSCSI. A LUN may be used with any device which supports read/write operations, such as a tape drive, but is most often used to refer to a logical disk as created on a SAN. Though not technically correct, the term "LUN" is often also used to refer to the logical disk itself.

IV. IMPLEMENTATION OF MULTIPLIER USING VM ALGORITHM

Multiplication methods are extensively discussed in Vedic mathematics. Various tricks and short cuts are suggested by VM to optimize the process. These methods are based on concept of

- Multiplication using deficits and excess.
- Changing the base to simplify the operation. Various methods of multiplication proposed in VM. Hence as follows.
  - UrdhvaTiryagBhyam - vertically and crosswise.
  - Nikhilam navatashcharamam Dashatah: All from nine and last from ten.
  - Anurupyena: Proportionately Vinculum

A. Urdhva Tiryagbhyam

Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. We discuss multiplicationo two, 4 digit numbers with this method [8-9].

B. Multiplier Architecture

The hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. Vedic Multiplier for 2x2 bit Module: The method is explained below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit Of the finel product.

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2]. Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier"s efficiency. Very precisely we can state that the total delay isonly 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in input, little modification is required.

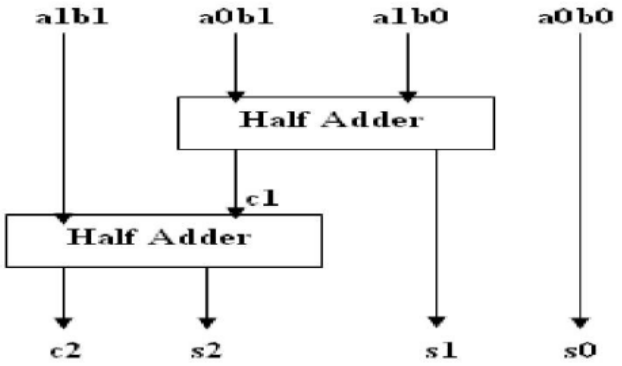

Fig.2.

V. RESULT

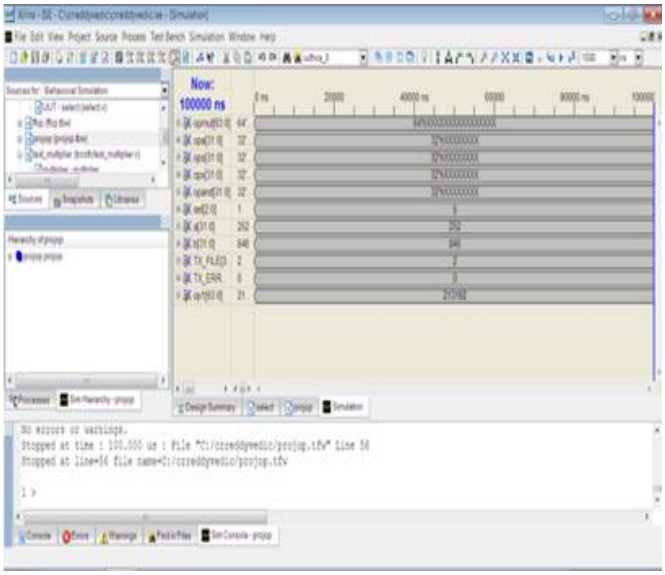

Fig.3.

RTL:

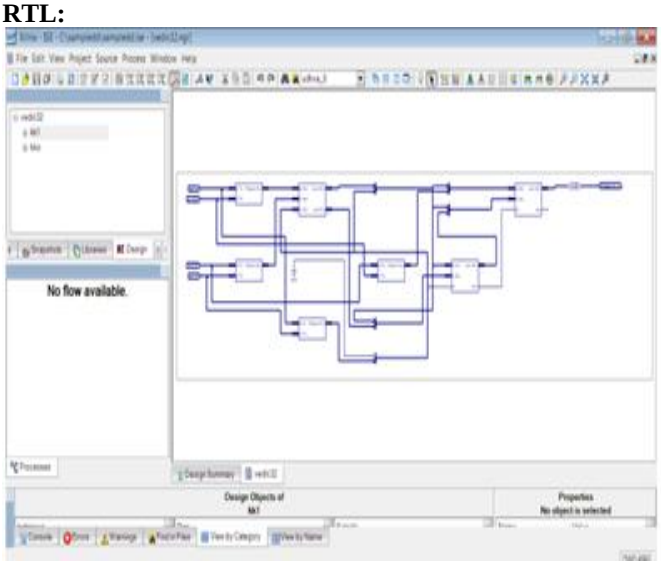

Fig.4.

VI. CONCLUSION

This paper presents a highly efficient method of ALU design. "Urdhva Tiryakbhyam Sutra" based on Vedic ALU. It is a method for hierarchical efficient ALU design which clearly indicates the computational advantages offered by Vedic methods. An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. We discussed a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers.

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