Implementation of Power Optimized MDC FFT Processor for MIMO-OFDM Systems using Reversible Logic

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Abstract: The architecture of multipath delay commutator (MDC) and memory scheduling are the basic concepts used to implement fast Fourier transform (FFT) processors with variable length. This FFT processors are used for multiple input multiple output-orthogonal frequency division multiplexing (MIMO-OFDM) systems. Depending on this MDC architecture, we implement the FFT/IFFT processor based design which is proposed in this paper. In this design we implement ram, fifo, input buffer and output sorting buffer. The adder operation is implemented using reversible logic HNG gate. The corresponding reversible logic is utilized in the RCA adder. So obviously the power consumption is reduced from 63.72mw to 13.24mw in the proposed implementation. The functionality verification and the synthesis is carried out using XILINX ISE 12.3i and shows the reduced delay values.

Keywords: Fast Fourier Transform (FFT), Memory Scheduling, Multiple-Input And Multiple-Output (MIMO), Orthogonal Frequency Division Multiplexing (OFDM), Output Sorting, Pipeline Based Multipath Delay Commutator (MDC), Wimax.

I. INTRODUCTION

When we require a data to be encoded at multiple frequencies then the popular scheme generally used is orthogonal frequency division multiplexing. This type of scheme is famous at wideband digital communication. Whether it may be wired or wireless such as television, broadcasting of audio, internet accessing, wireless networks and is widely used in latest technology like 4G mobile communication. Digital multi carrier modulation technique is used for OFDM. When we require to carry parallel streaming of data, a large spaced orthogonal sub-carrier signals are used in which each sub-carrier undergo convolution modulation like quadrature amplitude modulation or phase shift keying. OFDM have capability of channel equalization because it uses slowly modulated narrow band signals instead of using one highly modulated wide band signal. Using OFDM, FFT can be implemented without loss in efficiency. Narrow band co channel interfacing becomes very robust using ofdm ,it is very less sensitive over time synchronization errors. These type of OFDM signals have broad range of usage in WLAN under the standard of 802.11a, and digital radio systems standards like DAB/ERUKA 147, Terristial Digital TV systems (DVB-T) and Terrestrial Digital mobile systems (DVB-T).

Fast Fourier transform are used to compute discrete Fourier transform and also for its inverse. These technique used to convert to signals from time to frequency domain and vice versa.fft makes numeric algorithm as simple such that it is used in image processing and signal processing applications. In previous DFT is existed, in which the fastness drawback has overcome by FFT. OFDM uses reverse fft and transmitter side and fft and the receiver side to perform modulation and demodulation efficiently. FFT with OFDM is used cpu like intel Pentium at 1.26GHZ frequency and is able to calculate a 8 192 fft with in 576µs using FFTW, and in cpu called intel Pentium M AT 1.6 GHZ frequency and able to within 387 µs. a compared to earlier generation cpu ,a wide range of fft-ofdm based cpu named intel core 2 duo which operates at3 Gz frequency and able to perform the operations at 96. MIMO-OFDM defines multi input and multi output orthogonal frequency division multiplexing which is dominated over 4G AND 5G wireless communications ,the word multi input and multi output defines which is capable of sending multiple signals over multi antennas and orthogonal frequency division multiple communication system without loss in realiability. In earlier mimo is used with a combination of time division multiple access ,code division multiple access ,but mimo with ofdm is much famous for its high data rate,high message deliver capacity ,high throughput ,for these reasons only it is familiar at wires LAN and some standard networks at mobile communications . In mdc based mimo-ofdm as the data size increases the memory size also increases rapidly ,but by using multipath delay commutator the data flow will be controlled in simplest manner.the main reason for implementing mimo based ofdm is for its simplicity and which makes the user data in to a closely spaced narrow sub channels in such to eliminates biger obstacles to increase reliability.
II FFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the most efficient and fast algorithms to calculate the Discrete Fourier Transform and Inverse Discrete Fourier Transform respectively. Fast Fourier Transform/Inverse Fast Fourier Transform is mostly used in many communication applications like Digital Signal Processing and the implementation of this is a growing research. From the last years, OFDM became an important one in FFT algorithms and is going to be implemented. The efficient multiple access method for Bandwidth in digital communications is OFDM (Engels, 2002; Nee & Prasad, 2000). Many of nowadays OFDM technique can be used in most important wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Digital Video Broadcasting (DVB) , Wireless Local Area Network (WLAN) , Wireless Metropolitan Area Network (WMAN) and Multi Band – OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, this method is also utilised in important wired applications like Asymmetric Digital Subscriber Line (ADSL) or Power Line Communication (PLC).

Wireless technologies have evolved remarkably since Guglielmo Marconi said that the ability of radio can provide good contact with the ships sailing in the English channel in 1894. New theories and applications of wireless technologies have been developed by hundreds and thousands of scientists and engineers through the world ever since. Wireless communications can be regarded as the most important development that has an extremely wide range of applications from TV remote control and cordless phones to cellular phones and satellite-based TV systems. It changed people's life style in every aspect. Especially during the last decade, the industry of mobile radio communication is growing exponentially with increasing rate, fueled by the digital and RF (radio frequency) circuits design, fabrication and integration techniques and more computing power in chips. This trend will continue with an even greater pace in the near future.

The advances and developments in the technique have partially helped to realize our dreams on fast and reliable communicating 'any time anywhere". But we are expecting to have more experience in this wireless world such as wireless Internet surfing and interactive multimedia messaging so on. One natural question is: how can we put high-rate data streams over radio links to satisfy our needs? New wireless broadband access techniques are anticipated to answer this question. For example, the coming 3G (third generation) cellular technology can provide us with up to 2Mbps(bits per second) data service. But that still does not meet the data rate required by multimedia media communications like HDTV (high-definition television) and video conference. Clearly all the performance improvement and capacity increase are based on accurate channel state information. Channel estimation plays a significant role for MIMO-OFDM systems. For this reason, it is part of my dissertation to work on channel estimation of MIMO-OFDM systems.

![Fig1. Internal Architecture of FFT/IFFT Processors.](Image)

![Fig2. Inverse Fourier Transform.](Image)
Multiple Input Multiple Output (MIMO) systems are devices that are used in wireless communication. These are devices consisting of array of transmitters and receivers. With MIMO device it is possible to obtain high data. Hence combination of MIMO and OFDM system provides efficient data rate and reliability in wireless communications. IEEE 802.16 WIMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard, which can provide a data rates from 30 to 40 megabit/sec. 3GPP (3rd Generation Partnership Project) is the recent evaluation in IEEE 802.16 WiMAX. The 3rd Generation Partnership Project initiative evolved from a strategic one, which is between Nortel Networks and AT&T Wireless. AT&T Wireless was operated an IS-136 (TDMA) wireless network in the United States in 1998. The RAM is changed to DRAM to reduce the run time memory by using the memory scheduling technique where 12 memory blocks are sufficient instead of 16. Nortel Networks Wireless, which is an R&D center in Richardson, Texas, the wireless division of Bell Northern Research developed a vision for "an all Internet Protocol (IP)" wireless network that is having the internal name "Cell Web". In the proposed design the ram is replaced by dynamic ram.

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. The multiple output Boolean function $F(x_1; x_2; \ldots; x_n)$ of n Boolean variables is called reversible if the number of outputs is equal to the number of inputs and any output pattern has a unique pre-image. The reversible HNG gate can work singly as a reversible full adder. If the input vector $IV = (A, B, Cin, 0)$, then the output vector becomes $OV = (P=A, Q=Cin, R=Sum, S=Cout)$. If we consider $d = 0$, then “R” is taken as SUM and “S” is considered as CARRY.

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction). Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder. The block diagram of 4-bit Ripple Carry Adder is shown here below.
K.H.K.PRASAD, Ch.SATISH

III. FFT PROCESSOR METHODS

Fast Fourier Transform (FFT) is an efficient algorithm proposed by Cooley and Tukey to compute Discrete Fourier transform (DFT) which converts time to frequency and reduces the time complexity to \(O(N \log 2N)\), where \(N\) denotes the size of FFT. When considering the alternate implementations, the FFT/IFFT algorithm should be chosen to consider the execution speed, hardware complexity, and flexibility and precision. Nevertheless, for real time systems the execution speed is the main concern. Several architectures have been proposed over the last 3 decades like: single memory architecture, dual-memory architecture, cached memory architecture, array architecture, and pipelined architecture for the purpose of hardware implementation, various FFT processors have been used mainly 2 types of architectures which are Memory based architecture and Pipeline based architecture. Memory based architecture cannot be parallelized where as the pipeline architecture can overcome the disadvantages of the former architecture. Pipelined architectures characterized by real time, non-stopping processing and present smaller latency with low power consumption which makes them suitable for most application.

Generally, the pipeline FFT processors are classified in two design- architectures. They are Single-path delay feedback (SDF) pipeline architecture and Multiple-path delay Commutator (MDC) pipeline architecture. Single path delay feedback (SDF) reduces amount of multipliers but it complicates the control mechanism and uses more memory resources whereas Multipath Delay Commutator saves more area,[5] and thus MDC is adopted as the hardware architecture. Multipath Delay Commutator (MDC) makes the feedback paths in to feed forward streams using switch boxes along with memory. In this paper Multipath Delay Commutator and memory scheduling is used to implement fast Fourier transform for multiple input multiple output orthogonal frequency division with variable length. The observation made on the listed architectures reveals that the delay feedback architecture is more efficient than the corresponding delay commutator in terms of memory utilization. For computation of FFT we need to use twiddle factor to multiply with input signals to obtain output, and for this a huge size of ROM is required to store twiddle factors which in turn increases the cost. Thus for further improvement, ROM-less FFT/IFFT processor which eliminates ROM”s that store twiddle factor is presented. The complex multipliers are used for this purpose and they perform shift-and-add operations, thus the processor uses a digital multiplier with 2 inputs and does not require any storage element like ROM, to store twiddle factor. Thus the proposed architecture also includes a reconfigurable complex constant multiplier to store twiddle factor instead of using ROM”s.

IV. RESULTS

![Fig5. RTL Schematic.](image)

![Fig6. Simulation Results.](image)

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<th>Table1. Power Comparison Table</th>
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<td>EXISTED POWER</td>
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<td>63.72</td>
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V. CONCLUSION

The proposed high speed MDC architecture and memory scheduling are very much suitable for FFT/IFFT processor in multiple input multiple output OFDM system, because the constant multipliers are used to store the twiddle factors instead of ROM, Which utilizes 100% area and reduces the delay. The functionality verification and the synthesis is carried out using XILINX ISE 12.3i and shows the reduced power values. The RAM is changed to DRAM to reduce the run time memory by using the memory scheduling technique.
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So in the EXISTED design POWER is 63.72mw, where as in the proposed design the POWER is 13.24mw with the device of xc6vsx475tl-1ff1156. This reduction is due to the usage of reversible logic gate HNG. From the comparison table it concluded that the proposed POWER is very less. That’s why it is used in the low power applications.

VI. REFERENCES